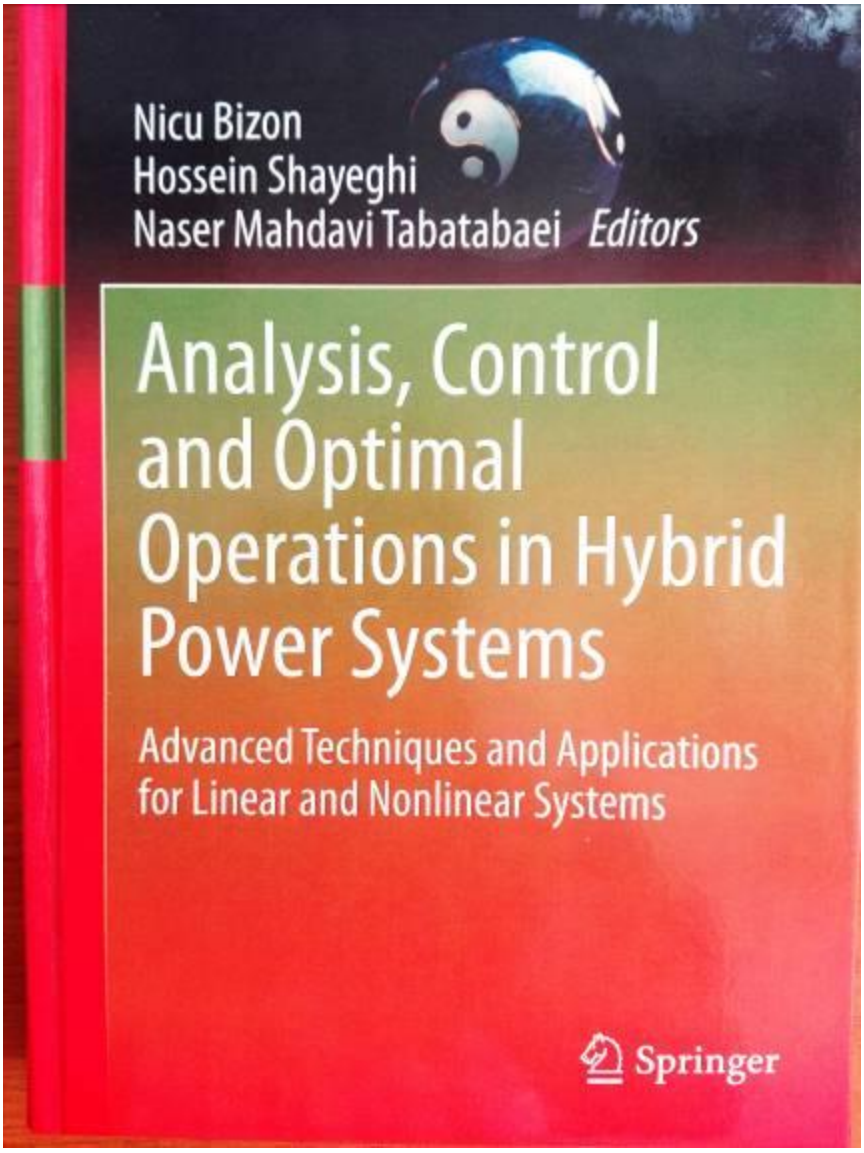
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7. Applications in Control of the Hybrid Power Systems

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Abstract: This chapter analyzes the control of the Hybrid Power Sources (HPS) based on some applications performed. Usually, a HPS combines two or more energy sources that work together with the Energy Storage Devices (ESD) to deliver power continuously to the DC load or to the AC load via the inverter system. In the automotive applications, the ESD stack can be charged from the regenerative braking power flow or from other power sources like the thermoelectric generator or the renewable source. The last may have a daily variable power flow such as the photovoltaic panels integrated into a car's body or into buildings. In the first section, an efficient fuel cell/battery HPS topology is proposed for high power applications to obtain both performances in energy conversion efficiency and fuel cell ripple mitigation. This topology uses an inverter system directly powered from the appropriate Polymer Electrolyte Membrane Fuel Cell (PEMFC) stack that is the main power source and a buck Controlled Current Source (buck CCS) supplied by a batteries stack, which is the low power auxiliary source. The buck CCS is connected in parallel with the main power source, the PEMFC stack. Usually, the FC HPS supply inverter systems and PMFC current ripple normally appears in operation of the inverter system that is grid connected or supply the AC motors in vehicle applications. The Low Frequency (LF) ripple mitigation is based on the active nonlinear control placed in the tracking control loop of the fuel cell current ripple shape. So, the buck CCS will generate an anti-ripple current that tracks the FC current shape. This anti-ripple current is injected into the output node of the HPS to mitigate the inverter current ripple. Consequently, the buck CCS must be designed in order to assure the dynamic requested in the control loop. The ripple mitigation performances are evaluated by some indicators related to the LF harmonics mitigation. It is shown that good performances are also obtained with the hysteretic current - mode control, but the nonlinear control has better performances. The nonlinear control of the buck CCS is implemented based on a piecewise linear control law. This control law is simply designed based on the inverse gain that is computed to give a constant answer for all levels of the LF current ripple. The con-

trol performances are shown by the simulations performed. Finally, the designed control law will be validated using a Fuzzy Logic Controller (FLC). In the second and the third section is proposed and analyzed a nonlinear control for FC HPS based on bi-buck topology that further improves FC performance and its durability in use in the low and medium power applications. The nonlinear voltage control is analyzed and designed in the second section using a systematic approach. The design goal is to stabilize the HPS output voltage. This voltage must have a low voltage ripple. Additionally, the power spectrum of this ripple must be spread in a wide frequencies band using an anti-chaos control. All the results have been validated with several simulations.

Keywords: Fuel cell, hybrid power sources, inverter systems, ripple mitigation, spread power spectrum, energy efficiency, nonlinear control.

7.1 INTRODUCTION

The PEMFC stack represents one of the most used solutions as main energy source in the Energy Generation Systems (EGS) and vehicle applications. This is due to its new performances in applications: small size, ease of construction, good energy efficiency, fast start-up and low operating temperature. Even if there are a lot of advantages in their using, the extensive use in such applications is unfortunately still limited due to their relatively short lifetime [1]. As it is known, the inverter current ripple is one of the main factors for low performances regarding the PEMFC energy efficiency [2; 3] and the PEMFC life cycle [4; 5; 6]. Also, it is known that the LF FC current ripple affects in much measure the PEMFC life cycle, causes hysteretic losses and subsequently more fuel consumption. The LF inverter current ripple contributes with up to 10% reduction in the available output power [7; 8]. Consequently, some limits for the LF FC current ripple or other slower load transients on different frequencies bands are specified. The FC stack has a rather large capacitance that can mitigate the High Frequency (HF) current ripple if the limits are not exceeded. Usually, only one limit for the HF ripple is specified.

The USA National Energy Technology Laboratory (NETL) published the first guidelines for the FC current ripple limits that can assure PEMFC stack operation without degradation of its performance [9]. The FC current ripple limits are given experimentally as values of the Ripple Factor (RF) measured for different frequency bands (for example, LF RF must be up to 5% from 10% to 100% load, but should not exceed 0.5 A for lighter loads; HF RF must be up to

40% from 10% to 100% load, but should not exceed 2 A for lighter loads). Lower values for the RF are certainly recommended to be obtained by an appropriate active control to further increase the PEMFC performances. For example, the interleaved control technique used in the parallel topology of the power converters supplied from the same PEMFC stack may be a solution for the FC current ripple mitigation [10; 11].

On the other hand, the slow FC power profiles (variations below grid frequency) represent the "load following" action of the EGS control and two control loops must be used: (1) the load following control loop will set the fuelling values according to the load requirements, and (2) the energy harvesting loop will use a Maximum Power Point (MPP) tracking technique to increase the energy amount extracted from the PEMFC stack in a real-time optimization manner. The MPP signal from the PEMFC should be tracked within 1% with a current-mode controller for purposes of both PEMFC reliability and efficiency [12; 13; 14].

In vehicle applications usually appear high energy demands that will cause high current slopes and obviously voltage drops, which are recognized as fuel starvation phenomenon. Consequently, it is necessary to add ESDs in the vehicles supplied by the PEMFC stack [15; 16; 17]. The ESDs having the short time response (for example the ultracapacitors stack) could be used as a Power Dynamic Compensators (PDC). Batteries and ultracapacitors are usually used as ESD's and PDC's, respectively. Those devices are used in the hybrid ESDs stack to compensate the fast power demand, reducing the FC starvation phenomenon by improving the dynamic performance of the HPS [18]. For the above considerations, it is obviously that the hybrid ESDs and fuel cell stacks need to be merged technologies in the HPS topologies. Usually, a HPS topology uses two or more energy sources and a hybrid ESD/PDC stack that work together as an embedded power unit (named as power hub) to deliver or store energy. Consequently, the challenge for the power management of the HPS is to enhance the performance of the entire HPS through these technologies working together [19]. The current slopes are given experimentally for different levels of the PEMFC stacks power (about 10 A/s per each kW of the rated power) [20; 21; 22]. Recently, some HPS topologies of FC/ultracapacitor type have been reported for vehicle applications [23], such as FC/battery HPS [24] and FC/ultracapacitor/battery HPS [8, 25]. In this chapter a FC/battery HPS topology is analyzed from the control point of view and behavior under dynamic load. The control goal is to mitigate the PEMFC current ripple as much as possible. Some ripple models for the PEMFC stack and appropriate power interfaces used to mitigate the FC current ripple are analyzed in [26; 27; 28, 29]. The state-of-art for the FC HPS topologies is presented in one of the chapters of this book, too.

In the first section, the analysis will be focused on modelling, designing and operating of the FC HPS with active control used to mitigate the inverter ripple based on a nonlinear control law. A high power FC/ESD/PDC HPS topology is proposed to obtain both performances in energy conversion and in ripple miti-

gation. This topology uses an inverter system that is directly powered from the appropriate FC stack and a buck CCS, which is also powered from the FC stack. In the next sections, a FC/ESD/PDC HPS structure based on the bi-buck topology is considered for medium power applications. The control goal for the buck CCS is the same: high mitigation of the FC current ripple based on an active control. The necessity of a nonlinear gain in the control loop is shown by simulation. After that, this control law is validated through a FLC that generates a 2-D control surface based on two input control variables: (1) the output voltage error and the FC current ripple. One of the contour projections for this 2-D control surface can be chosen as a nonlinear control law. On the other hand, the control goal for the buck Controlled Voltage Source (CVS) is to stabilize the HPS output voltage having a low voltage ripple that is spread in wide frequencies band. The simulation results successfully show that nonlinear voltage control performs good performances in the frequency-domain (high spreading level of the power spectrum) and in the time-domain (low RF level of the output voltage), too. Conclusions are given in the last section.

7.2 PROBLEM STATEMENT AND USED MODELS

In order to estimate the inverter current ripple using the Matlab-Simulink® toolboxes, some simulations are made for the inverter systems of mono-phase and three-phase type. The obtained results are shown in one of the chapters of this book. The LF current ripple of the input inverter current is back propagated from load to the DC output of the HPS via the inverter system. Obviously, the power spectrum of the current ripple has the HF harmonics situate at multiples of the carrier frequency, but their levels are much smaller than the levels of the LF harmonics. The HF harmonics were generated by the switching action of the inverter system. Usually a PWM pure sine command is used, having the carrier frequency in range of 10 kHz to 100 kHz.

As it was known, the main harmonic for the grid-connected mono-phase inverters is situated at twice of the grid frequency and the significant LF harmonics are situates at multiples of this harmonic. If the grid frequency is of 50 Hz, then the significant LF harmonics are situates at frequencies of 100 Hz, 200 Hz and 300 Hz. Also, for the grid-connected three-phase inverters, the main harmonic is situated at triple of the grid frequency. Thus, the significant LF harmonics are situates at frequencies of 150 Hz, 300 Hz and 600 Hz. If the mono- and three-phase inverter supply an AC load (for example, an electrical AC machine), then the main harmonic is situated at twice or triple of the working frequency and the significant LF harmonics are situated at multiples of it. Those results obtained (namely the spectral distribution observed for the LF harmonics of the current ripple, and the observed levels of these harmonics in simulations and experiments performed) will be considered in designing an equivalent load

for the inverter system behaviour. The equivalent load is implemented by a CCS having the control signal a superposition of three rectified sine wave with frequency of 50 Hz, 150 Hz and 300 Hz. Also, the levels for these harmonics can be set independently. Those levels are set to 30 A, 5 A and 5 A for case shown in Fig. 7.1. The HF current ripple is not considered in the load model because the PEMFC stack has a high tolerance to it. The DC reference current, $I_{HPS(base)}$, will be chosen in correlation with the MPP of the used PEMFC stack (see Fig. 7.1 and 7.2).

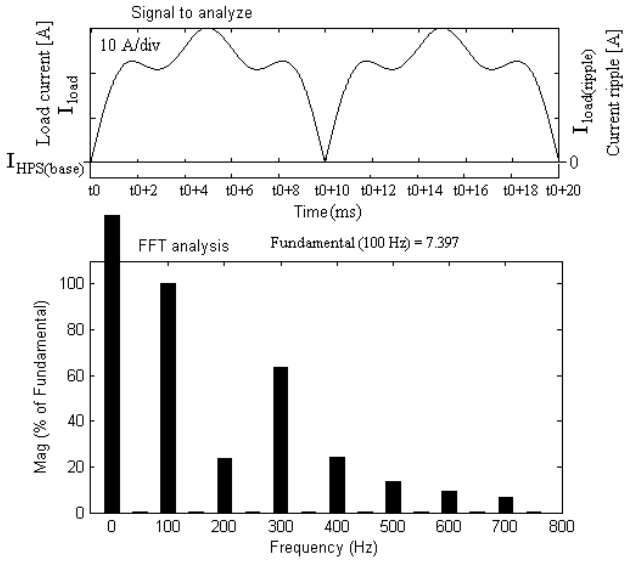


Fig. 7.1. The equivalent load current (top) and its power spectrum (bottom); adapted from [35]

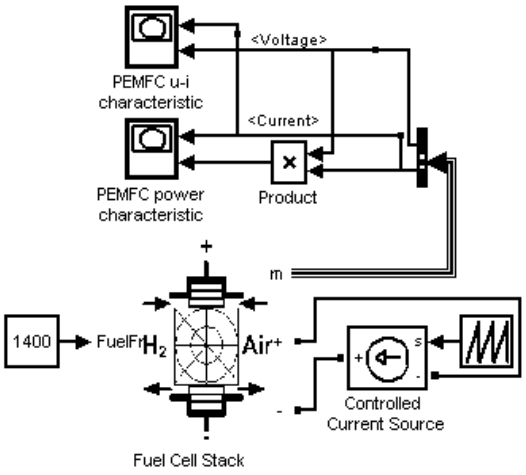


Fig. 7.2. The Simulink diagram used to obtain the static characteristics of the PEMFC stack used

Three types of PEMFC stack will be used in simulation: one for high power applications and two for medium power applications. Also, two type of batteries stack will be used in accordance with the power level of application implemented. This statement is also valid for used type of ultracapacitors stack.

Next subsections will briefly present the HPS models and the parameters values set for the PEMFC model used.

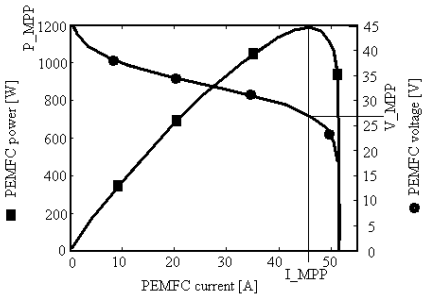
7.2.1 Fuel cell model

Some detailed PEMFC models are now available in literature [30; 31, 32]. One that combines in a well manner the PEMFC operating relationships is now available in Matlab - Simulink®.

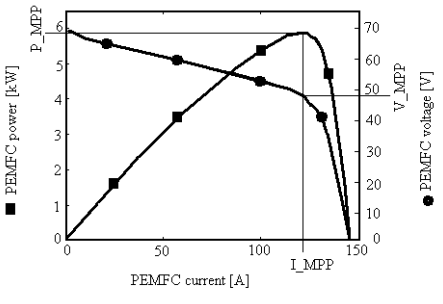
Three preset PEMFC models are used in this chapter, having the main parameters specified below [33, 34, 35]:

- 1.26 kW PEMFC stack that for a FuelFr=10.5 lpm will have the MPP at approximately at 45 A and 27 V (Fig. 7.3.a);
- 6 kW PEMFC stack that for a FuelFr=47 lpm will have the MPP approximately at 120 A and 50 V (Fig. 7.3.b).
- 50 kW PEMFC stack that for a FuelFr=1400 lpm will have the MPP approximately at 240 A and 560 V (Fig. 7.3.c).

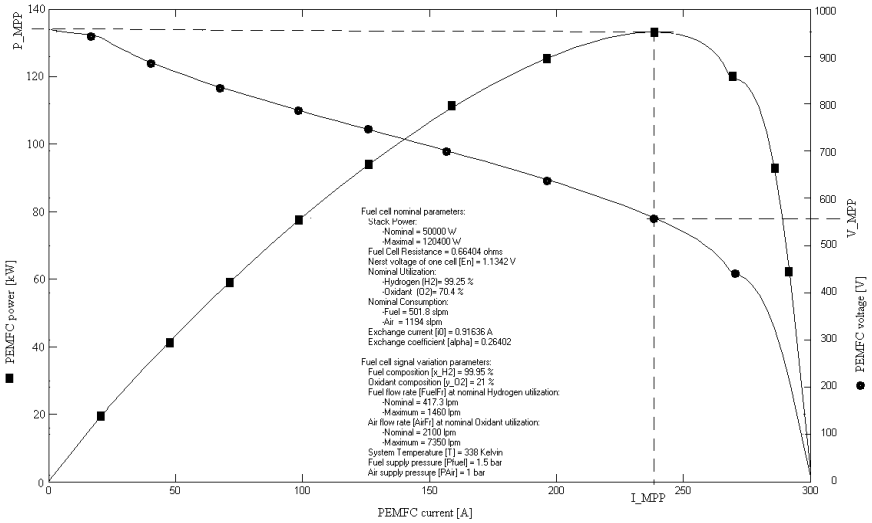
Other parameters of the preset model for the used Fuel flow rate (named FuelFr and measured in litres per minute, lpm) are shown in Fig. 7.3, too.



a) 1.26 kW PEMFC static characteristics at the fuel flow rate of 10.5 lpm



b) 6 kW PEMFC static characteristics at the fuel flow rate of 47 lpm



c) 50 kW PEMFC static characteristics at the fuel flow rate of 1400 lpm

Fig. 7.3. The PEMFC static characteristics; adapted from [33, 35]

7.2.2 Energy storage devices models

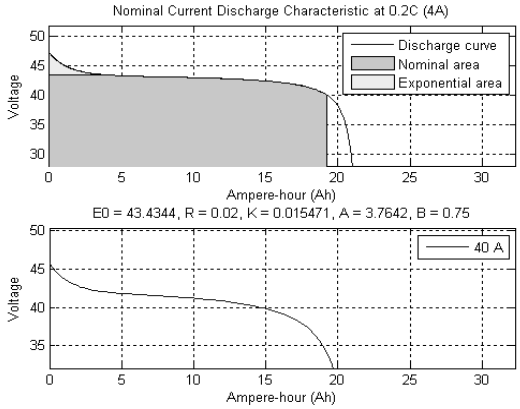
Usually, the medium power FC HPS topologies use a power interface based on the MPP tracking control to extract the maximum energy from the PEMFC stack via a grid-connected inverter. Off-grid power systems also use MPP tracking controller to harvest the energy from the PEMFC stack. The power delivered by the FC HPS must always be bigger than the needed load power. The flow rate regulator (which is driven by the FC current) control the power delivered by the PEMFC to assure this requirement until the maximum available FC power. In the transitory regime, when the load power requirements are less or greater than the power currently available (which must always be near the MPP), the power difference is delivered by an auxiliary energy source (wind turbine or/and photovoltaic panel) or an ESD (usually a batteries stack). If the CVS controller sets a constant voltage in the HPS output node, then the energy management based on the power balance implies an ESD current controlled by the CCS controller. The buck CCS extracts the necessary energy from the ESD in order to compensate the sharp power profiles for the dynamic loads (the power difference that appears for short time in output node). A PDC stack (usually an ultracapacitors stack) is used directly (in parallel with the PEMFC stack) or via a bidirectional DC-DC power converter.

If a bi-buck topology is used, then the HPS output voltage will be lower than the PEMFC voltage at MPP. This value was chosen to be 25 Vdc and 40 Vdc for the case of using the 1.26 kW and 6 kW PEMFC stack, respectively. The batteries stacks were chosen in relation with those voltage values. Detailed models for battery are now available in literature [35] and one generic is now available in Matlab - Simulink®, too. A preset NiMH battery model will be used. For the preset model the model parameters based on the battery type, nominal voltage value and the rated capacity are used. The initial State-Of-Charge (SOC) is set to 80% in all simulations. The used parameters are specified below for each PEMFC's stack:

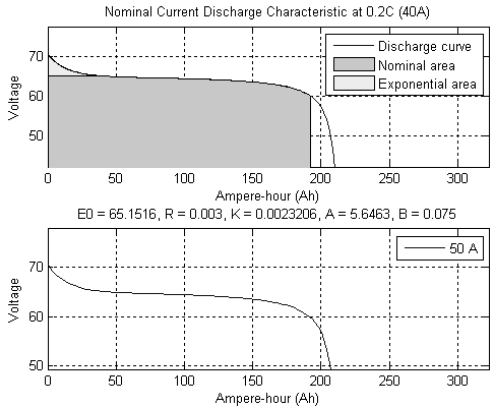
- For the 1.26 kW PEMFC: the NiMH battery parameters are set to 40 V and 20 Ah for the nominal voltage and rated capacity, respectively (see discharge characteristics on Fig. 7.4.a);
- For the 6 kW PEMFC: the NiMH battery parameters are set to 60 V and 200 Ah for the nominal voltage and rated capacity, respectively (see discharge characteristics on Fig. 7.4.b).
- For the 50 kW PEMFC: the NiMH battery parameters are set to 800 V and 100 Ah for the nominal voltage and rated capacity, respectively (see discharge characteristics on Fig. 7.4.c).

The set values are chosen to obtain a reasonable value for the duty cycle of the PWM command applied to the buck CCS.

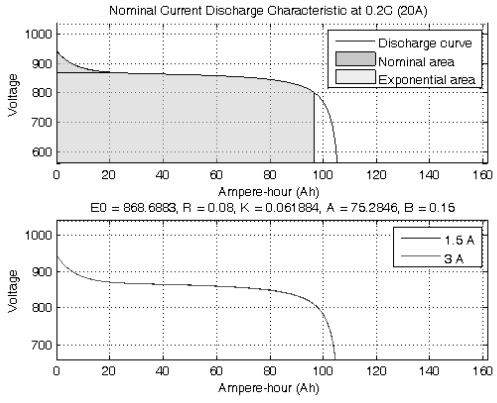
Batteries technology represents a good option to be used as ESD in different power applications, while the ultracapacitors technology represents an attractive option to be used as PDC in burst power applications.



a) 20 Ah (40 V) NiMH battery



b) 200 Ah (60 V) NiMH battery



c) 100 Ah (800 V) NiMH battery

Fig. 7.4. The NiMH battery discharge characteristics; adapted from [33]

The ultracapacitors stack provides the difference between the load demand and the power delivered by the PEMFC/battery hybrid system. In this chapter a PEMFC/ultracapacitors /battery hybrid system is adopted. The capacitance value used for the ultracapacitors stack depends on the imposed HF voltage ripple, the switching frequency and the load power level. A first order model is used to model the ultracapcitors stack.

7.2.3 Load test model

It is obvious that the LF ripple current appears on the HPS DC voltage bus in the same way for all multi-phase inverter systems topologies. Consequently, the equivalent load for the inverter system was implemented by a CCS that is controlled to cover all these cases. The control signal can be a superposition of three rectified LF sine waves having different levels for these LF harmonics.

The levels for the LF harmonics of 50 Hz, 150 Hz and 300 Hz are set at 30 A, 30 A and 5 A for the example shown in Fig. 7.5. The DC reference current, $I_{HPS(base)}$, defines the base level from which the current ripple shall be deemed (see Fig. 7.1 and 7.5).

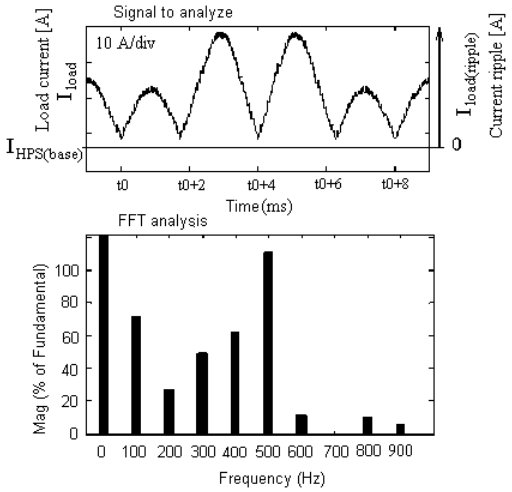


Fig. 7.5. The load current (top) and its power spectrum (bottom); adapted from [33]

As it was mentioned before, the current slopes are given experimentally for different power of the PEMFC stacks, and the recommended value is 10 A/s per each kW power. So, the recommended limit for the PEMFC stacks considered is of 12 A/s, 60 A/s and 500 A/s, respectively. The maximum current slope is higher than·20 A/ms (2000 A/s) for the both current load shapes shown in Fig. 7.1 and 7.5. So, it is much higher than the admissible FC current slope. If a ripple of 30 A_{p-p} (peak-to-peak value) is considered for the load current, then the

RF value for the PEMFC stacks considered, $RF_{load\_current}$, will be about of 30 A / 45A = 75.5 %, 30 A / 120 A = 25 % and 30 A / 240 A= 12.5 %, respectively. Thus, the RF for the load current was set high enough to show the performances of the ripple mitigation for the HPS under proposed control. Of course, all the above can be easily changed by using a new set of parameters for the equivalent load. Values used in the simulation will be mentioned in each case.

It can be noted that if the ripple mitigation loop operates, then the buck CCS will compensate the main part of this ripple and the rest will propagate back to the PEMFC stack. Moreover, this remaining ripple can be spread in a large HF band through the anti-chaos control of the CVS (see the last section of this chapter). Consequently, the both LF and HF $RF_{PEMFC\_current}$ values will be lower than the recommended limits. Considering a current slope higher than 20 A/ms, it is obvious that these parameters of the load model will ensure an unacceptable dynamic for the PEMFC stack. So, the dynamic of the HPS power flows must be compensated via a buck CCS converter. Further details about the HPS operation will be shown in the modelling section of the bi-buck HPS topology and the appropriate control section

7.3 NONLINEAR CONTROL OF THE HIGH POWER FC HPS

This section is organized as follows. The issues of high-power HPS topologies based on PEMFC stack as main energy source are presented in the first subsection. Some simulation results for the FC HPS that supplies an inverter system or an equivalent load are shown in the second subsection. The necessity to have a nonlinear gain in the control loop is analyzed in the third subsection. Its design is shown, too. The possibility to design this nonlinear control law by a fuzzy logic controller is shown in the fourth subsection. Last subsection concludes this section.

7.3.1 The high-power HPS topology

The EGS architecture with the mitigation control for the FC current ripple is shown in Fig. 7.6. The topology of the buck CCS and the structure of its controller are shown in Fig. 7.7 and 7.8. The modelling of the FC/battery HPS topology and the design of the nonlinear law control that can replace the linear gain, G_{Ifc}, are presented in [35]. The low-pass filter inductance, L_f, is used to connect in parallel the PEMFC stack and the buck CCS. Because the ripple of the FC current, I_{FC}, without use of the buck CCS, and the anti-ripple generated by the buck CCS current, I_{CCS}, will have almost the same magnitude, L_f value could be equal to the buck CCS inductance, L_{buck} (for example, $L_f = L_{buck}$=100 μH). The L_f inductance and the internal capacitance of the PEMFC stack forms a low-pass filter that mitigates the HF current ripple. The C_f capacitor is used to obtain the imposed RF of voltage on the HPS DC bus (usually, $C_f > 100$ μF).

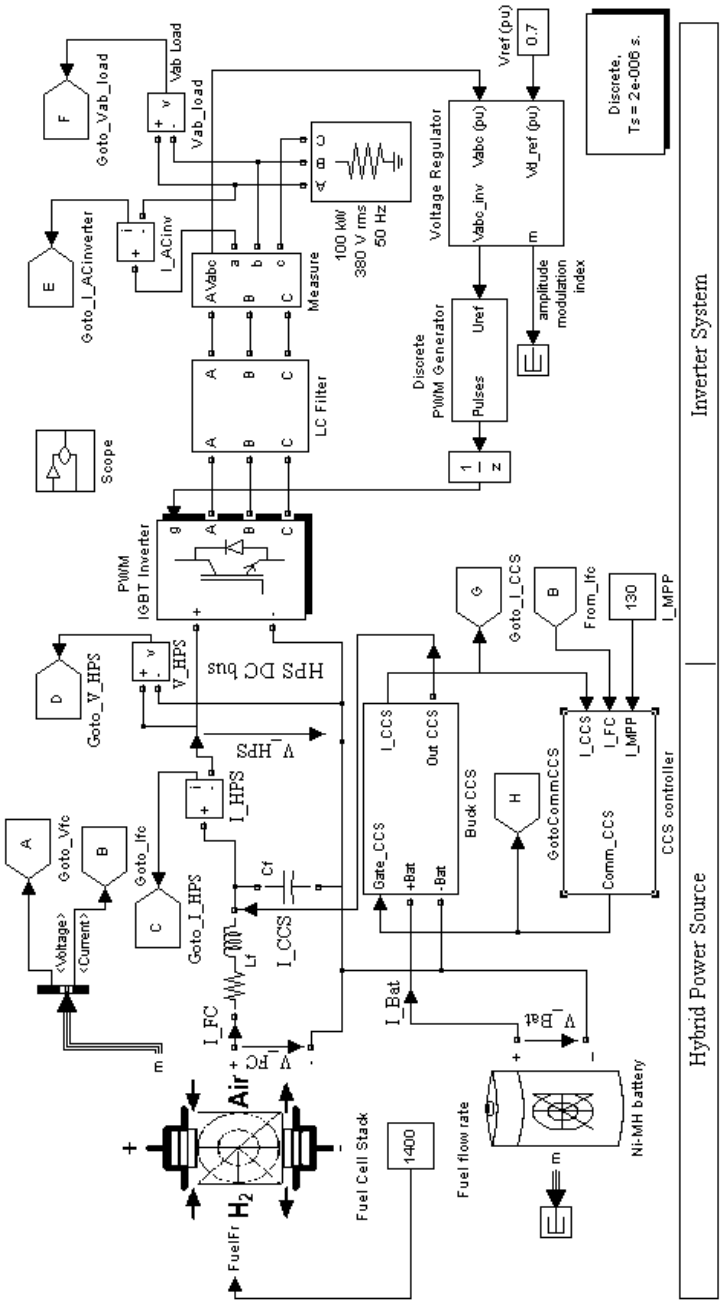


Fig. 7.6. The EGS architecture that use a FC/battery HPS topology having a control loop to mitigate the FC current ripple; adapted from [33, 35]

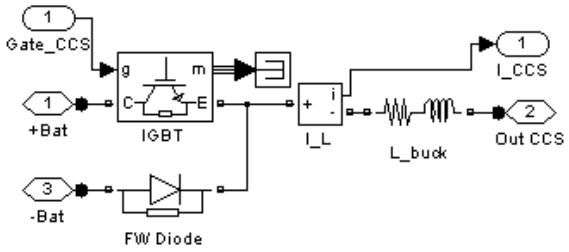


Fig. 7.7. The structure of the buck CCS

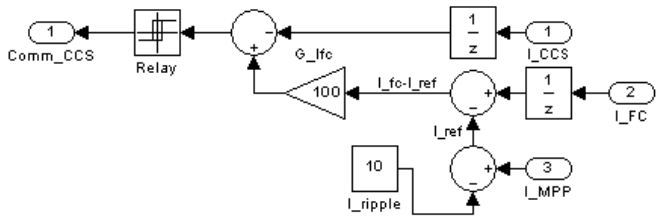


Fig. 7.8. The structure of the CCS controller [35]

The value of the L_{buck} inductance must be chosen small to assure a short time response of Buck CCS, but large enough to operate it in the current continuous mode (for example, $50 < L_{buck}$ [μH] < 150 if a 6 kW PEMFC stack is used and the load ripple is 30 A_{p-p}) [26]. The mitigation control loop must have a short time response to better track the shape of the inverter current ripple. So, a value close to the minimal value (also named as critical value) must be used. However, note that a too low value could increase the HF ripple over the imposed limits. The HF ripple magnitude dependents on the hysteresis value that is set for the relay block (see Fig. 7.8). So, the hysteresis value was chosen to obtain a HF ripple up to the imposed limits. Considering the simplicity of the circuit design, the hysteretic control was chosen to be used as a current-mode control method. The switching frequency for the buck CCS will be in range of 5 kHz to 50 kHz if 10 Amps is used for the hysteresis value. The G_{Ifc} gain value set the mitigation performance, defining the tracking accuracy of the ripple shape for the inverter current that is propagated back to the PEMFC stack. Thus, the buck CCS will generate an I_{CCS} current, which is in fact an anti-ripple that will be injected in the HPS output node to mitigate the inverter current ripple. The anti-ripple will be generated based on the gained FC ripple (not based on the gained inverter ripple) to reduced the HF ripple in the FC ripple. Also, it is obvious that both FC and inverter ripples have the same LF shape in the FC EGS architecture without current ripple mitigation control (Fig. 7.9). This architecture without current ripple mitigation control is used to compare the mitigation performances.

The FC HPS topology that is shown in Fig. 7.10 has an equivalent load that replaces the inverter system.

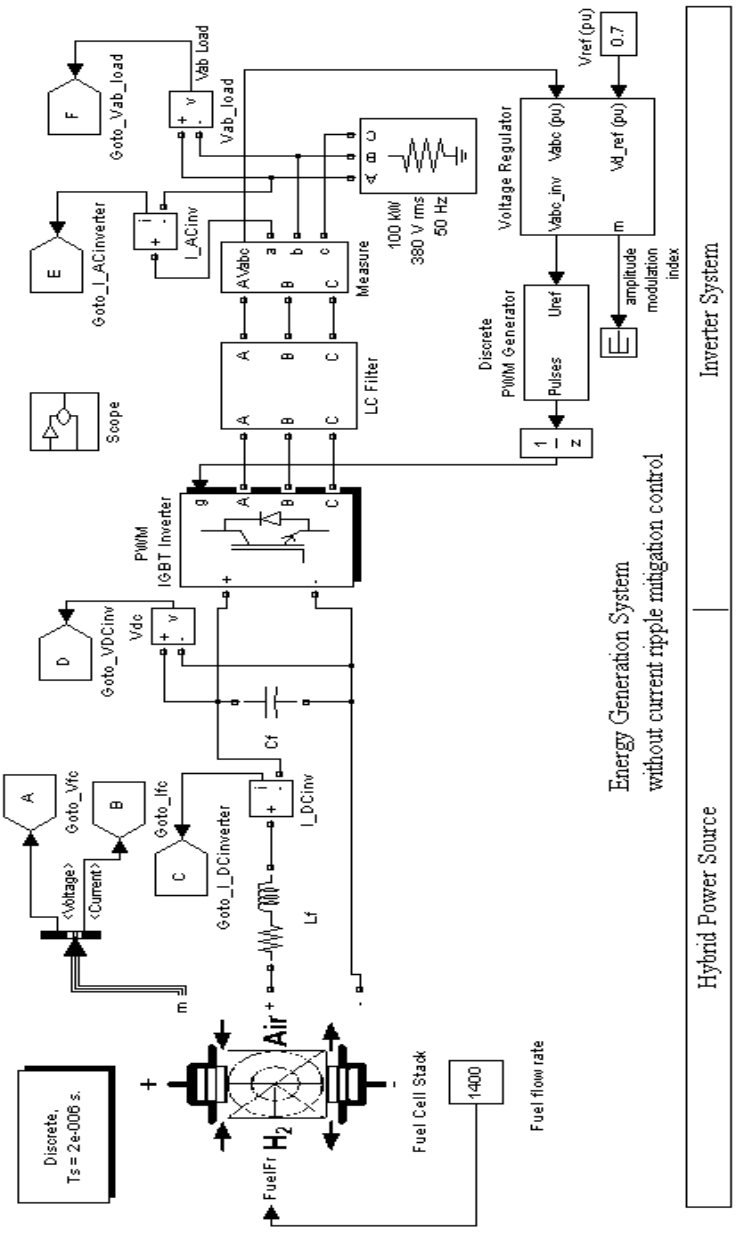


Fig. 7.9. The FC EGS architecture without current ripple mitigation control

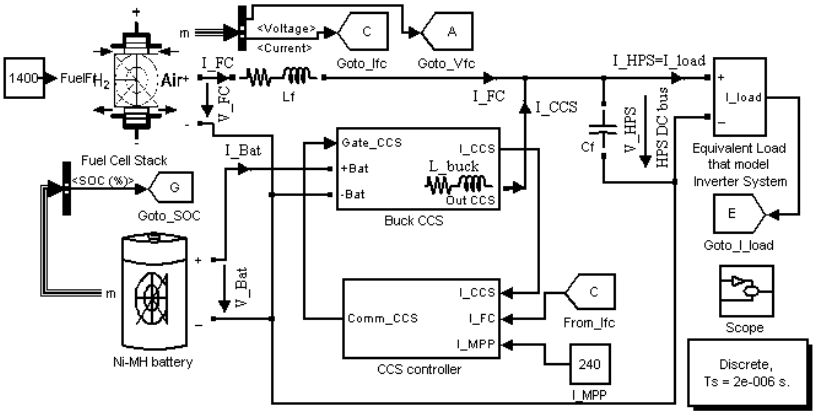


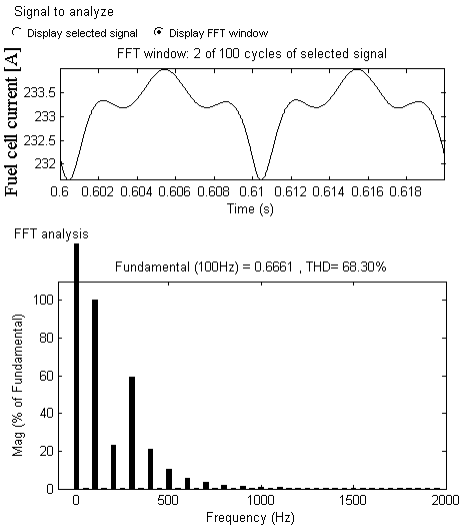
Fig. 7.10. The FC HPS topology with a current ripple mitigation control and equivalent load

As it was mentioned, the use of an equivalent load instead of the inverter system will speed-up simulation, without affecting the analysis of the mitigation performances that is performed in the LF range for different shapes of ripples.

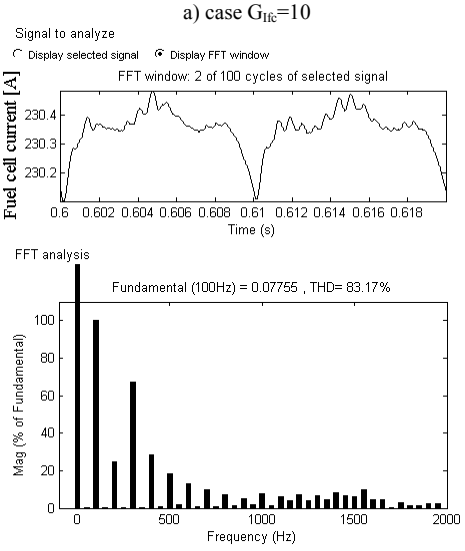
7.3.2 Simulation results

Some simulation results considering the FC EGS architecture, with and without control feature to mitigate the inverter ripple, are shown in Fig. 7.11 and 7.12. The shape of the buck CCS current will track the LF shape of the input inverter current (Fig. 7.12.b). This is put in evidence by the magnitudes of the LF harmonics, which are almost the same for the both currents [35]. The LF harmonics magnitudes of the FC current for two G_{Ifc} gains are shown in Fig.7.11. Note that the 100 Hz harmonic magnitude decreases from 0.6661 A for G_{Ifc}=10 (Fig. 7.11.a) to 0.07755 A for G_{Ifc}=100 (Fig. 7.11.b), but not in a linear manner. Further simulations performed showed that the mitigation ratio is not linear vs. the G_{Ifc} gain, which vary in range 1 to 100 [35]. The mitigation ratio is computed as ratio of the ripples in the HPS and the FC outputs. The mitigation ratio could be also computed as ratio of RF values, RF_{HPS} / RF_{FC}, considering that average values are almost equal for the FC and the HPS currents. In the same manner the mitigation ratios for different LF harmonics can be defined. For example, the load current for the equivalent load shown in Fig. 7.1 has the base value, $I_{HPS(base)}$, 240 A , the ripple peak-to-peak 30 $A_{p\text{-}p}$, and the 100 Hz harmonic magnitude 7.397 A. Thus, the mitigation ratio of the 100 Hz harmonic is about 7.397/0.6661 ≅ 11.1 and 7.397/0.07755 ≅ 95.4 for case of G_{Ifc}=10 and G_{Ifc}=100, respectively.

The effective mitigation ratio of the 100 Hz harmonic is about 0.1629/0.07755 ≅ 2.1 for G_{Ifc}=100 (see Fig. 7.11.b and Fig. 7.12.a). Also, the effective mitigation ratios for the 300 Hz and 600 Hz harmonics are about 2.1·165/65 ≅ 5.3 and 2.1·45/17 ≅ 5.6, respectively.



a) case G_{Ifc}=10



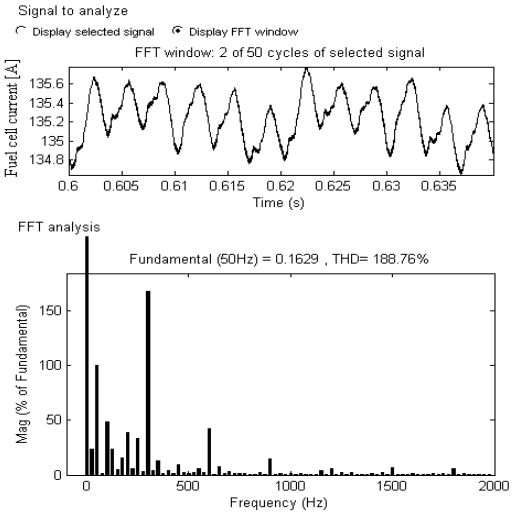
b) case G_{Ifc}=100

Fig. 7.11. The simulation results for the FC EGS architecture with current ripple mitigation control

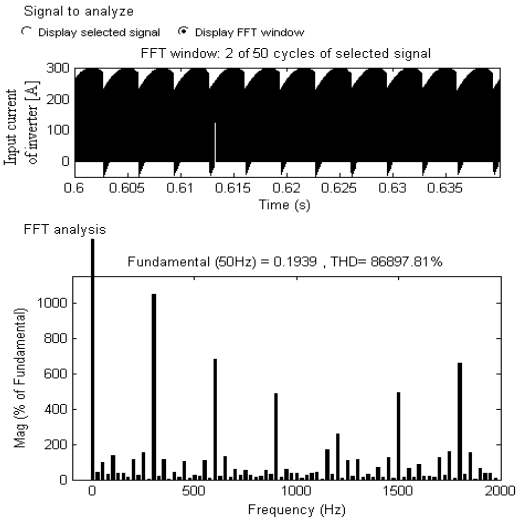
7.3.3 The design of the nonlinear control law based on simulation results

The characteristic of the FC current ripple vs. G_{Ifc} gain is shown in Fig. 7.13.a. It is obvious that this is a nonlinear law. The ripple mitigation ratio, RM,

is defined as a ratio of the load current ripple and FC current ripple, $RM=\Delta I_{load}/\Delta I_{FC}$.



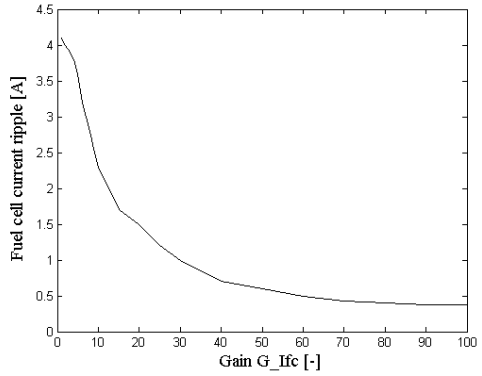
a) The fuel cell current ripple (top) and its power spectrum (bottom)



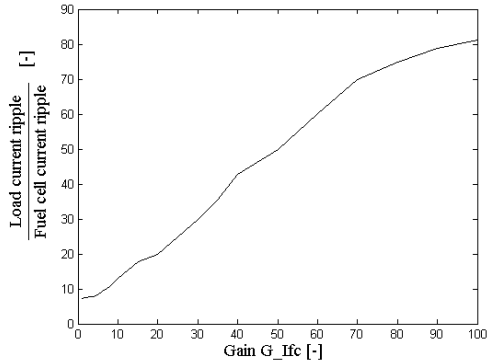
b) The input inverter current (top) and its power spectrum (bottom)

Fig. 7.12. The simulation results for the FC EGS architecture without current ripple mitigation control

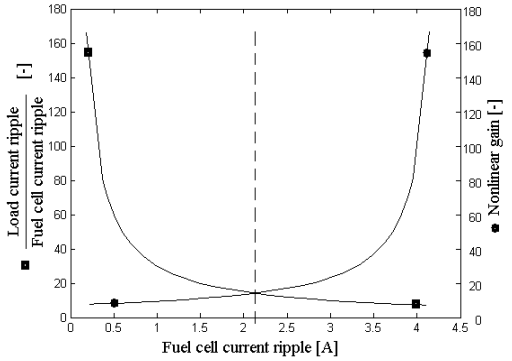
The characteristic of the RM vs. the G_{Ifc} gain is shown in Fig. 7.13.b.



a) FC current ripple vs. G_{Ifc} gain



b) RM vs. G_{Ifc} gain



c) RM vs. FC current ripple

Fig. 7.13. The performance characteristics of the FC HPS topology with current ripple mitigation control [35]

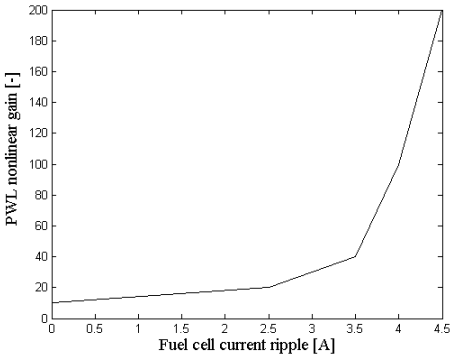
Consequently, the characteristic of the Ripple mitigation ratio, RM, vs. the FC current ripple can be computed, as it is shown in Fig. 7.13.c (marker ■),

considering different G_{Ifc} gain in range. If the control goal is to have a ripple mitigation almost constant for different load current ripple, then the G_{Ifc} must have the shape of the nonlinear gain (marked with ● in Fig. 7.13.c) that is symmetrically against vertical axis (the dashed line).

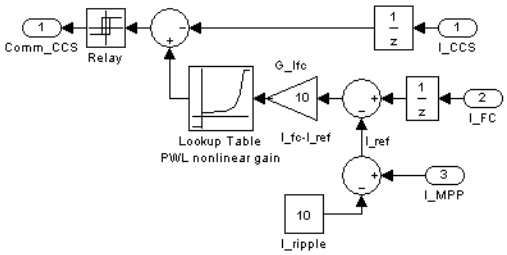
This nonlinear gain could be simply implemented by a piecewise linear (PWL) function, using for example a look-up table (see Fig. 7.14.a):

X = [0, 2.5, 3.5, 4, 4.49, 4.5] and Y = [10, 20, 40, 100, 200, 200].

The PWL nonlinear gain is shown in Fig. 7.14. The nonlinear CCS controller structure is shown in Fig. 7.14, too. The control gain has a nonlinear part (the PWL nonlinear gain) and a linear part (G_{Ifc}), that increases the mitigation performance by choosing a gain value in range 1 to 10. Note that a higher value than 10 will increase the switching frequency over 50 kHz [35].



a) PWL nonlinear gain



b) The structure of the nonlinear CCS controller [35]

Fig. 7.14. The nonlinear CCS controller

Simulation results for the FC HPS topology with the CCS nonlinear controller that uses a PWL nonlinear gain are extensively presented in [35]. For example, the ripple mitigation ratio of the 100 Hz harmonic value is about 7.397/0.032 ≅ 231, so its effective RM will be about 231/95.4 ≅ 5.1. The nonlinear control goal is validated based on the simulations performed for all the LF harmonics, resulting that the effective RM has almost the same value [35].

7.3.4 The design of the nonlinear law based on a fuzzy logic controller

The nonlinear control law will be also designed through a FLC to validate the obtained RM characteristic vs. the FC current ripple. If the G_{Ifc} constant gain is set to 10, then the X vector will be scaled with 10 and renamed as Xg. Consequently, the nonlinear gain that includes both constant and variable gains can be implemented by the following PWL function:

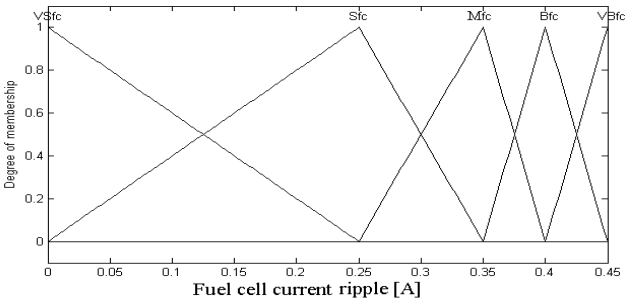
Xg = [0, 0.25, 0.35, 0.4, 0.449, 0.45] and Y = [10, 20, 40, 100, 200, 200].

The methodology to design the FLC is detailed in [34]. The shapes of the memberships functions that result for the FC current ripple (fc), the ripple mitigation ratio (rm), which are the input variables, and the output command signal (com) are shown in Fig. 7.15, plot a, b and c, respectively. Five membership functions are defined for both input variables in correlation with pair of vectors (Xg, Y). These are named as VS=Very Small, S=Small, M=Medium, B=Big and VB=Very Big. It can be observed that their peaks are located at values of the Xg and Y vectors. Also, five membership functions are uniformly defined for the output variable in range 0 to 1. They are named as VS=Very Small, S=Small, M=Medium, B=Big and VB=Very Big.

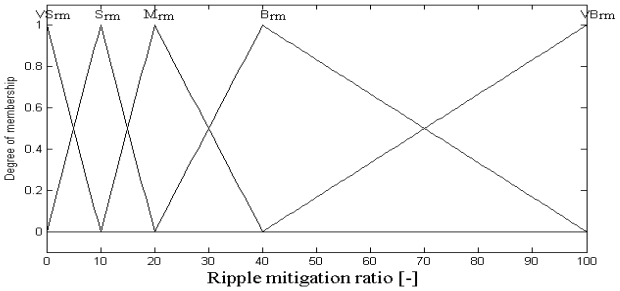
The rules base is shown in Table 7.1. The proposed CCS controller that uses this FLC is shown in Fig. 7.15.d. The Mamdani implication and center of gravity defuzzification method are used. The resulting control surface and the contour projections for different levels of the command signal are shown in Fig. 7.15, plot e and f, respectively. It can be observed that the projection contour of the 0.7 level is so similar with the shape of the PWL nonlinear gain shown in Fig. 7.14.a, considering the constant gain, G_{Ifc}=10, ie using the pair of vectors (Xg, Y). This result validates the previous design made through the trial and the error method using the simulation results. The 0.7 level will be set for the threshold of the relay used to convert the FLC output into a PWM command. A 0.2 hysteresis is set for the same relay.

Table 7.1. FLC rules base [35]

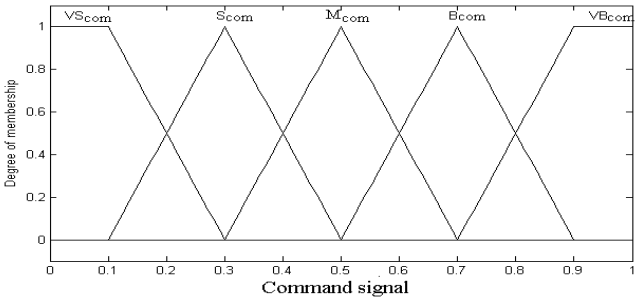
Command signal		Fuel cell current ripple [A]				
		VSfc	Sfc	Mfc	Bfc	VBfc
Ripple mitigation	VSrm	Mcom	Scom	VScom	VScom	VScom
	Srm	Bcom	Mcom	Scom	VScom	VScom
	Mrm	VBcom	Bcom	Mcom	Scom	VScom
	Brm	VBcom	VBcom	Bcom	Mcom	Scom
	VBrm	VBcom	VBcom	VBcom	Bcom	Mcom



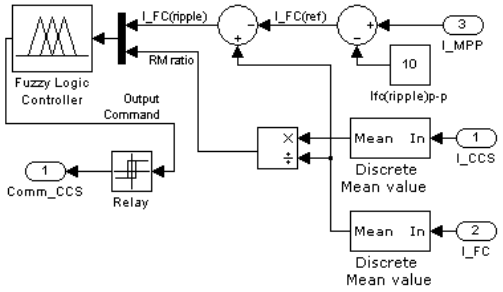
a) Fuel cell current ripple memberships



b) Ripple mitigation ratio memberships

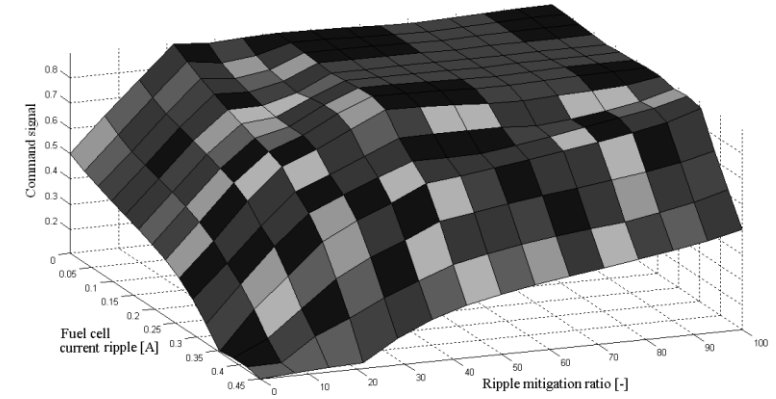


c) Command signal memberships

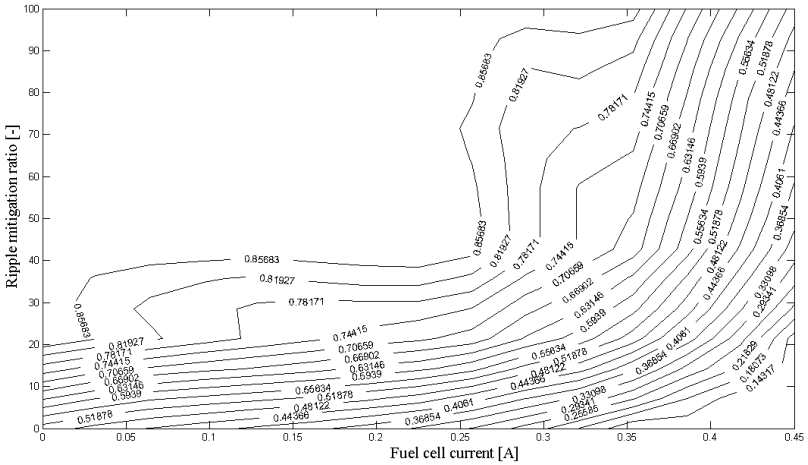


d) CCS controller using a FLC

Fig. 7.15. Design of the FLC for the CCS controller [35]



e) FLC control surface



f) Contours of the FLC control surface

Fig. 7.15. The design of the FLC for the CCS controller [35] (continued)

As a conclusion, in this section a systematic design of a nonlinear controller is presented. Two ways to design the nonlinear control law are proposed. The first one is based on simulations to draw the characteristic of the ripple mitigation ratio vs. the FC current ripple. The nonlinear control law is designed by symmetry. The second one is based on the FLC control surface. The 0.7 – cut of this surface is projected in plane of the input variables, defining almost the same nonlinear control law.

7.4 NONLINEAR CONTROL OF MEDIUM POWER FC HPS

Some interesting control solutions to mitigate the FC current ripple are presented in [7, 36, 37] for medium power FC HPS. The FC power is considered constant, near to MPP, and this operating regime will be set in the proposed HPS topology shown in Fig. 7.16.a. The HPS topology proposed is based on a bi-buck structure. Using an appropriate control the FC current ripple is mitigated and spread in wide frequency band. This section is organized as follows. The first subsection briefly presents the HPS proposed. Modelling and designing of the HPS based on bi-buck topology are shown in the second subsection. Designing of the proposed nonlinear law for current and voltage control is presented in subsection 3 and 4, respectively. Some selected simulation results are shown, too. The last subsection concludes this section.

7.4.1 The medium-power HPS topology

As it is known, the boost or full-bridge converter topologies are suitable to boost the FC voltage and to mitigate the FC current ripple with appropriate control [7, 36, 37], but here a bi-buck topology will be used [38]. One of the buck converters will operate as CVS, while the other will operate as CCS. The buck CCS will generate an anti-ripple via the tracking control implemented in the CCS controller to mitigate the load current ripple. The buck CCS will operate as an active LF ripple filter, spreading the LF ripple in wide frequency band via the anti-control scheme implemented in the CVS controller. The CVS controller must assure a stabilized output voltage, V_{out}, too. So, the voltage error will be used as an input. An anti-control scheme to chaotify the switching command of a buck converter is proposed in [39]. In this way, the remained LF ripple power spectrum is spread in the HF band, increasing the PEMFC life cycle. Consequently, the HPS power interface has two control loops: one for adjusting the output voltage at the imposed value by the reference voltage, V_{ref}, and other for mitigating the LF current ripple through compensation. A nonlinear control of the voltage-mode and the current-mode will be designed for this power interface. The HPS power interface based on a bi-buck topology is shown in Fig. 7.16.b.

The current ripple mitigation technique proposed in [40] is tested here by simulation. The nonlinear controller law is designed by the trial and the error method. Also, this innovative bi-buck converter topology is proposed in [33, 34] as a multi-port power interface (see Fig. 7.17) and its appropriate voltage- and current-mode control will be further analyzed in the next sections.

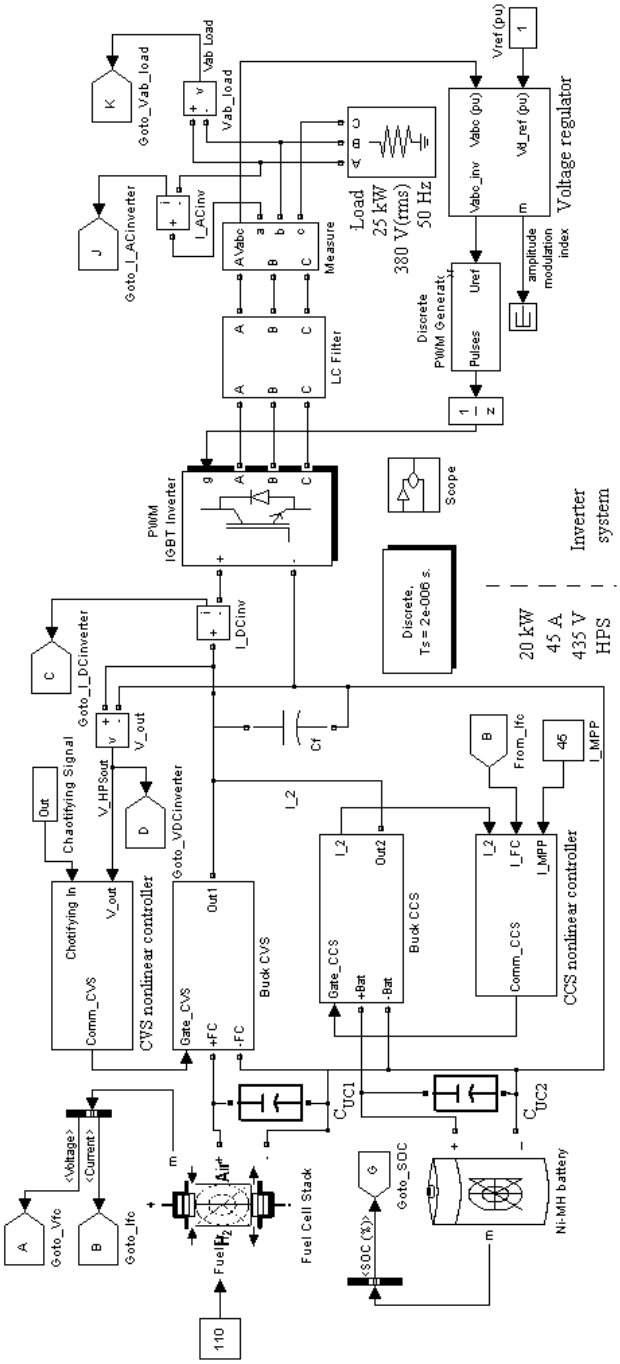


Fig. 7.16.a. A three-phase inverter system (with pure sine PWM command) powered by the 20 kW (435 V, 44 A) HPS

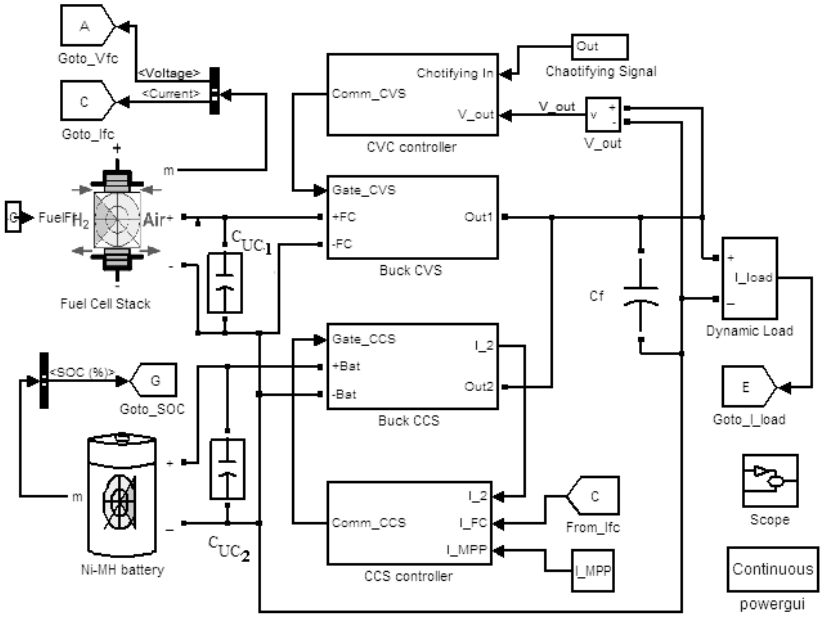


Fig. 7.16.b. The bi-buck HPS topology [33]

7.4.2 Modeling and designing of the HPS power interface

For a 1.26 kW HPS (1.26 kW PEMFC/ 1 F ultracapacitor / 20 Ah NiMH battery) the design parameters are set to $V_{out} \cong V_{ref}=25V$, $I_{FC(AV)} \cong I_{MPP}=45A$ (so, $V_{FC(MPP)} \cong 27V$ based on FC characteristic), $V_{Bat}=40V$ and the profile of the load current was shown in Fig. 7.5. These parameters will be considered below in the HPS design. The load current, i_{out}, is given by relationships written based on average (AV) and alternative (AC) components:

$$i_{out} + i_{Cf} = i_1 + i_2 \Rightarrow \begin{cases} I_{out(AV)} = I_{1(AV)} + I_{2(AV)} \\ i_{out(AC)} + i_{Cf(AC)} = i_{1(AC)} + i_{2(AC)} \end{cases} \quad (1)$$

If the output voltage ripple is considered small, then the AC current through the filtering capacitor, $i_{Cf(AC)}$, will be much lower than the AC load current, $i_{out(AC)}$:

$$i_{1(AC)} + i_{2(AC)} = i_{out(AC)} + i_{Cf(AC)} \cong i_{out(AC)} \quad (2)$$

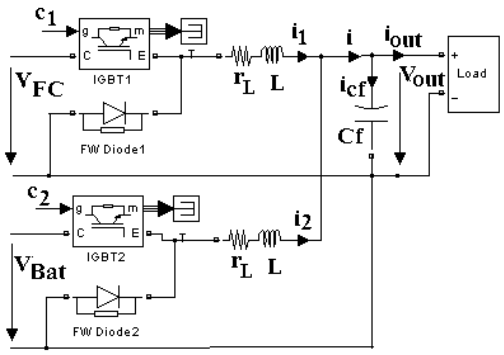


Fig. 7.17. The HPS power interface of bi-buck type; adapted from [33, 34]

If the LF current ripple compensation control loop operates correctly, then $i_{1(AC)} << i_{2(AC)}$, too, resulting:

$$\begin{aligned} & i_{2(AC)} \cong i_{out(AC)} \\ & I_{2(AV)} = I_{out(AV)} - \frac{\eta_1 V_{FC(MPP)}}{V_{out}} \cdot I_{MPP} \end{aligned} \tag{3}$$

where η_1 is the energy efficiency of the buck CVS. This is calculated as the ratio between the output power (delivered to the load) and the input power (delivered by the PEMFC stack).

Because the unidirectional CCS topology is cheaper than a bidirectional CCS topology, the first topology was considered here. Consequently, the relationships for the AC components must be redefined in terms of a positive ripple. If a base current is defined as a value slightly smaller than the minimum value of the respective current (as it is shown in Fig. 7.5 for the load current, i_{out}), then the difference from the base current can be defined as a positive ripple. Consequently, the above relationships may be rewritten as:

$$\begin{cases} i_{out} = I_{out(base)} + i_{out(ripple)} \\ i_2 = I_{2(base)} + i_{2(ripple)} \end{cases} \Rightarrow \begin{cases} i_{2(ripple)} \cong i_{out(ripple)} \\ I_{2(base)} = I_{out(base)} - \dfrac{\eta_1 V_{FC(base)}}{V_{out}} \cdot I_{FC(base)} \end{cases} \tag{4}$$

where $I_{FC(base)} \cong I_{MPP} - I^*_{FC(ripple)p\text{-}p}$, and $I^*_{FC(ripple)p\text{-}p}$ is the FC current ripple (peak to peak) without the buck CCS.

Based on this definition the PEMFC current does not exceed I_{MMP}, even if the compensation loop is not yet in the operating phase or it is accidentally malfunctioned. If $I^*_{FC(ripple)p\text{-}p} \cong 10\%\ I_{MPP}$ is chosen, then the base operating point is $I_{FC(base)} \cong 40$ A (where $V_{FC(base)} \cong 33$ V). In this case all HPS operating phases are

carried out normally (without exceeding the allowable limit parameters) and the PEMFC base operating point is still close enough to the MPP. If the compensation loop starts to operate, then the anti-ripple is generated in the range defined by the gap chosen towards the MPP. The energy delivered by the auxiliary power source (for example, a batteries stack) is minimized if the base current, $I_{2(base)}$, is set to be zero (or slightly greater than zero). In this case:

$$I_{out(base)} \cong \frac{\eta_1 V_{FC(base)}}{V_{out}} \cdot I_{FC(base)} = I_{1(base)} \tag{5}$$

Considering $\eta_1 \cong 0.9$, then $I_{out(base)} \cong 48$ A. Also (see Fig. 7.5):

$$I_{2(AV)} \cong I_{2(ripple)(AV)} \cong I_{out(ripple)(AV)} \approx 23A \tag{6}$$

Considering $\eta_2 \cong 0.9$ (where η_2 is the power efficiency of the buck CCS), then:

$$I_{Bat(AV)} \cong \frac{V_{out}}{\eta_2 V_{Bat}} \cdot I_{2(AV)} \approx 16A \tag{7}$$

As it was mentioned before, the current levels of the batteries stack could be temporally higher than this minimum level that is computed with Eq. 7, due to the relatively large response time of the FC stack. In this transitory regime of the FC stack, the supplementary power flow is supplied via the buck CCS from the batteries stack. If it is necessary, a mixed batteries and ultracapacitors stack may be used to assure high energy demands in a short time. Of course, it is necessary to have a small response time for the buck CCS, too. Generally, the basic PWM converters (like buck, boost, and buck-boost topologies) are second-order systems, in which one state variable is the inductor current and the other state variable is the capacitor voltage (which is also equal to the output voltage). Of course, the bi-buck HPS topology (see Fig. 7.17) can be modelled by a third-order system that usually uses as state variables the filtering capacitor voltage (which is equal to the output voltage) and both inductor currents. It will be shown below that the HPS topology can be also modelled by second-order systems, if the load power profile is given by the load current modelled through a CCS. Modelling analysis is focused on the current-mode control of the buck CCS that can compensate the inverter current ripple via the anti-ripple generated by the buck CCS. The DC components and the LF components are of interest in designing the current-mode control [14]. Consequently, the LF components are used to characterize the buck CCS dynamic and the proposed model tries to emulate the behaviour of the bi-buck converter in the LF range.

If c1 and c2 are switching command for the IGBT transistors ($c_1=1/0 \Rightarrow$ $IGBT_1$ on/off and $c_2=1/0 \Rightarrow$ $IGBT_2$ on/off), then (neglecting the series resistance of the inductors and filter capacitor) the operating equations are:

$$\begin{aligned} c_1 v_{FC} &= L_1 \frac{di_1}{dt} + v_{out} \\ c_2 v_{Bat} &= L_2 \frac{di_2}{dt} + v_{out} \\ i_1 + i_2 &= i_{out} + i_{Cf} \\ i_{Cf} &= C_f \frac{dv_{out}}{dt} \end{aligned} \tag{8}$$

With a simple manipulation of the equations above, a second-order differential equation is obtained:

$$\frac{L_2}{L_1 + L_2} c_1 v_{FC} + \frac{L_1}{L_1 + L_2} c_2 v_{Bat} = \frac{L_1 \cdot L_2}{L_1 + L_2} \frac{di_{out}}{dt} + v_{out} + C_f \cdot \frac{L_1 \cdot L_2}{L_1 + L_2} \frac{d^2 v_{out}}{dt^2} \tag{9}$$

Considering identical inductors (L_1 =L_2 =L, having the same series resistance, r_L), the second-order differential equation (9) can be rewritten as:

$$\frac{1}{2}\left(c_1 V_{FC} + c_2 V_{Bat}\right) - \frac{r_L}{2} i_{out} - \frac{L}{2} \frac{di_{out}}{dt} = V_{out} + \frac{C_f r_L}{2} \frac{dv_{out}}{dt} + \frac{C_f L}{2} \frac{d^2 v_{out}}{dt^2} \tag{10}$$

where the second-order system parameters are the natural frequency, ω_n [rad/s], and the dimensionless damping ratio, ξ:

$$\omega_n = \sqrt{\frac{2}{C_f L}}, \quad \xi = \frac{C_f r_L}{4} \omega_n = \frac{r_L \sqrt{2}}{4} \sqrt{\frac{C_f}{L}} \tag{11}$$

As it was mentioned above, this model can show the output voltage dependence to the load current. If series resistance of the inductor, r_L, and of the filter capacitor, r_C, will be considered in modelling, then the operating equations are:

$$\begin{aligned} c_1 v_{FC} &= r_L i_1 + L \frac{di_1}{dt} + v_{out} \\ c_2 v_{Bat} &= r_L i_2 + L \frac{di_2}{dt} + v_{out} \\ i_1 + i_2 &= i = i_{out} + i_{Cf} \\ v_{out} &= r_C i_{Cf} + \frac{1}{C_f} \int i_{Cf} dt \end{aligned} \tag{12}$$

The model of the HPS system is obtained by summing the first two relations in (11). If the voltage of FC and batteries stacks will be considered almost con-

stant during a LF period ($dv_{FC}/dt \cong 0$ and $dv_{Bat}/dt \cong 0$; see Fig. 7.18), then, by differentiating the last relationship, a second-order differential equation is obtained, too:

$$\frac{1}{2}\left(c_1 v_{FC} + c_2 v_{Bat}\right) - v_{out} = \frac{r_L}{2} i + \frac{L}{2}\frac{di}{dt} \Rightarrow 0 \cong \frac{dv_{out}}{dt} + \frac{r_L}{2}\frac{di}{dt} + \frac{L}{2}\frac{d^2 i}{dt^2} \tag{13}$$

The second-order differential equation for the filtering current, i_{Cf}, is obtained by differentiating the last two relations of (12) and then using them in (13):

$$\left.\begin{aligned} \frac{di}{dt} &= \frac{di_{out}}{dt} + \frac{di_{Cf}}{dt} \\ \frac{i_{Cf}}{C_f} + r_C \frac{di_{Cf}}{dt} &= \frac{dv_{out}}{dt} \end{aligned}\right\} \Rightarrow \begin{aligned} &-\frac{r_L}{2} C_f \frac{di_{out}}{dt} - \frac{L}{2} C_f \frac{d^2 i_{out}}{dt^2} \cong \\ &\cong i_{Cf} + \left(\frac{r_L}{2} + r_C\right)\frac{di_{Cf}}{dt} + \frac{L}{2} C_f \frac{d^2 i_{Cf}}{dt^2} \end{aligned} \tag{14}$$

The switching frequency is chosen to be in a range of approximately 10 kHz value and the designed range for the filtering capacitor is from 10 μF to 100 μF.

Neglecting the series resistor of the capacitor, the amplitude (peak-to-peak) of the filtering current can be estimated by using the last equation of (8):

$$I_{Cf(p-p)} \cong C_f f_s V_{FC} \cdot RF_V \tag{15}$$

where RF_V is the voltage ripple factor defined for the output voltage:

$$RF_V = \frac{\Delta v_{out}}{V_{out}} \tag{16}$$

The design goal for the CVS controller is to obtain a $RF_V < 4\%$ using a filtering capacitor in range from 10 μF to 100 μF.

The amplitude of the filtering current is about 0.6 and 2 A for the test loads considered (Fig. 7.1 and 7.5, respectively). Thus, the assumption regarding the level of the filtering current was correct (see last relation of (1)). This assumption mentions that this current is smaller than the ripple of the output current, so:

$$i = i_{out} + i_{Cf} \cong i_{out} \tag{17}$$

If the LF range is considered to be from 50 Hz to 1000 Hz, then the time of a ripple pulse, $2\Delta t_p$, (named above as a LF period) will be in range from 1 to 20 ms (see Fig. 7.19 and Fig. 7.20). The voltages of both FC and batteries stacks and also output voltage can be considered constant during this short time:

$$v_{out} \cong V_{out}, \; v_{FC} \cong V_{FC}, \; v_{Bat} \cong V_{Bat} \tag{18}$$

Also, the voltage over the series resistor of the inductor is much smaller than the output voltage:

$$\frac{r_L}{2} i_{out} << V_{out} \tag{19}$$

Taking into account these assumptions, the first two relations of (8) can be rewritten. Summing both relations, the relation that can model the HPS behaviour in all operation phases will be obtained (see Fig. 7.18):

$$\frac{\left(c_1 V_{FC} + c_2 V_{Bat}\right)/2 - V_{out}}{L/2} = \frac{di_{out}}{dt} = \frac{di_{out(ripple)}}{dt} \tag{20}$$

The CVS starts to operate after the start-up phase of the PEMFC stack, when the PEMFC voltage becames bigger than the output voltage reference, $V_{ref(out)}$. In all this time the load is powered via the CCS. If the CVS starts to operate, then the FC stack current appears. The mitigation phase starts when the FC stack current become bigger than $I_{FC(base)}$ value. From now on, the load is mainly powered via the CVS and the load ripple will be mitigated via the CCS. During this phase both converters operate and four states of the transistor's conduction appear (see Table 7.2).

For each conduction state, the current slope for the output current can be estimated using the equation (20), as below:

$$\begin{aligned} s_1 &= \frac{\Delta i_{out(I)}}{t_{on1on2}} \cong \frac{\left(V_{FC} + V_{Bat}\right)/2 - V_{out}}{L/2}; \quad s_2 = \frac{\Delta i_{out(II)}}{t_{on1off2}} \cong \frac{V_{FC}/2 - V_{out}}{L/2} \\ s_3 &= \frac{\Delta i_{out(III)}}{t_{off1on2}} \cong \frac{V_{Bat}/2 - V_{out}}{L/2}; \quad s_4 = \frac{\Delta i_{out(IV)}}{t_{off1off2}} \cong \frac{-V_{out}}{L/2} \end{aligned} \tag{21}$$

The relationship that gives the LF ripple amplitude of the load pulse is:

$$\Delta I_{out(ripple)} = n_1 s_1 t_{on1on2} + n_2 s_2 t_{on1off2} + n_3 s_3 t_{off1on2} + n_4 s_4 t_{off1off2} \tag{22}$$

If both converters normally operate, then the same equation (20) is operational, considering:

$$v_{out} \cong V_{out} \cong V_{ref(out)}, \; v_{FC} \cong V_{FC(base)}, \; v_{Bat} \cong V_{Bat(base)} \tag{23}$$

Table 7.2: The conduction states of the HPS operation during the startup of the mitigation phase [34]

State	C1	C2	The duration of state [s]	The current slope [A/s]	The average number of switching periods into a state
I	1	1	t_{on1on2}	s_1	n_1
II	1	0	$t_{on1off2}$	s_2	n_2
III	0	1	$t_{off1on2}$	s_3	n_3
IV	0	0	$t_{off1off2}$	s_4	n_4

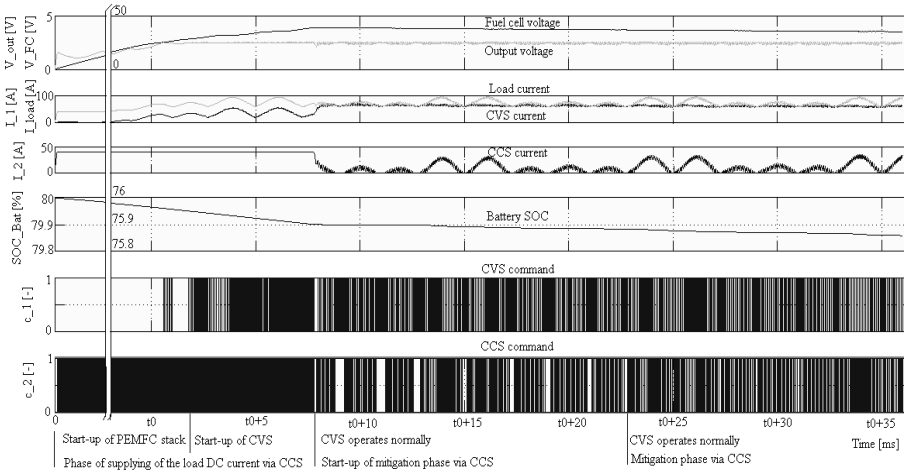


Fig. 7.18. The HPS behaviour powered by 6 kW PEMFC [34]

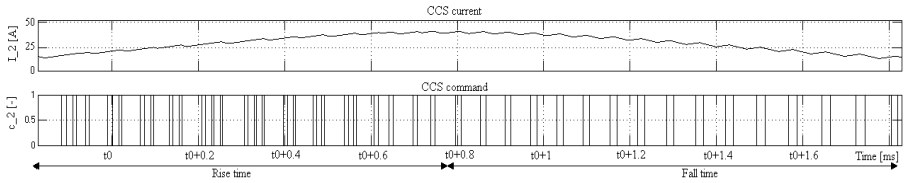


Fig. 7.19. Zoom of the buck CCS behaviour during the mitigation phase (6 kW PEMFC case) [34]

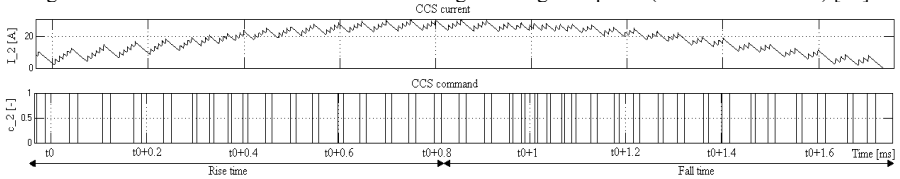


Fig. 7.20. Zoom of the buck CCS behaviour during the mitigation phase (1.26 kW PEMFC) [34]

During the mitigation phase, the buck CCS generates an anti-ripple current that makes an active compensation of the output current ripple. In this HPS operation regime, the buck CCS behaviour can be shown using the second relationship of (8):

$$\frac{c_2 V_{Bat} - V_{out}}{L} \cong \frac{di_2}{dt} = \frac{di_{2(ripple)}}{dt} \cong \frac{di_{out(ripple)}}{dt} \tag{24}$$

A zoom of the buck CCS current shape is shown in Fig. 7.19 and 7.20 for the HPS powered by a 6 kW and 1.26 kW PEMFC stack, respectively. A pulse of the LF buck CCS current shape has a rise time (Δt_r) and a fall time (Δt_f). During the rise and fall time phase the buck CCS current rises to $\Delta I_{out(rise)}$ value and falls from $\Delta I_{out(fall)}$ value. The positive and negative slopes are (see also the Table 7.3):

$$s_5 = \frac{\Delta i_{2(r)}}{t_{on2(r)}} = \frac{\Delta i_{2(f)}}{t_{on2(f)}} \cong \frac{V_{Bat} - V_{out}}{L}; \quad s_6 = \frac{\Delta i_{2(r)}}{t_{off\,2(r)}} = \frac{\Delta i_{2(f)}}{t_{off\,2(f)}} \cong \frac{-V_{out}}{L} \tag{25}$$

Table 7.3. The CCS behaviour during the mitigation phase [34]

CCS current [phase]	C2	The average time of each phase [s]	The current slope [A/s]	The average number of switching periods into a phase
Rise	1	$t_{on2(r)}=T_2D_{2r}$	s_5	n_r
Rise	0	$t_{off2(r)}=T_2(1-D_{2r})$	s_6	n_r
Fall	1	$t_{on2(f)}=T_2D_{2f}$	s_5	n_f
Fall	0	$t_{off2(f)}=T_2(1-D_{2f})$	s_6	n_f

In this phase, when both converters operate normally, the behaviour of the buck CVS can be shown using relationships (8). The converters operate independently to satisfy the control goals under the switching command generated by each controller (see Fig. 7.21). The simulation results shown in Fig. 7.18 are obtained using a hysteretic current-mode control. In the next section the simulation results will be also shown for a constant frequency method, the peak-current-mode control (PCC) method.

Some design relationships will be written below. For example, the ripple amplitude for the buck CCS current during the rise phase is about:

$$\Delta I_{out(rise)} = n_r (s_5 t_{on2(r)} + s_6 t_{off\,2(r)}) = n_r T_2 [s_5 D_{2r} + s_6 (1 - D_{2r})] \tag{26}$$

Consequently, the average number of the switching periods into the rise time phase is:

$$n_r \cong \frac{\Delta t_r}{T_2} \cong \frac{\Delta I_{out(rise)}}{T_2 [s_5 D_{2r} + s_6 (1 - D_{2r})]} \tag{27}$$

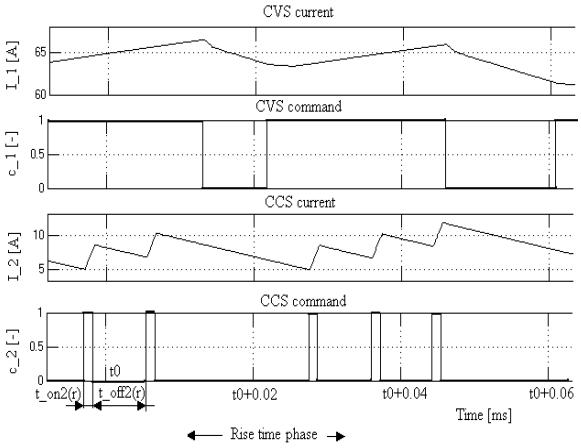


Fig. 7.21a. 1.26 kW PEMFC case

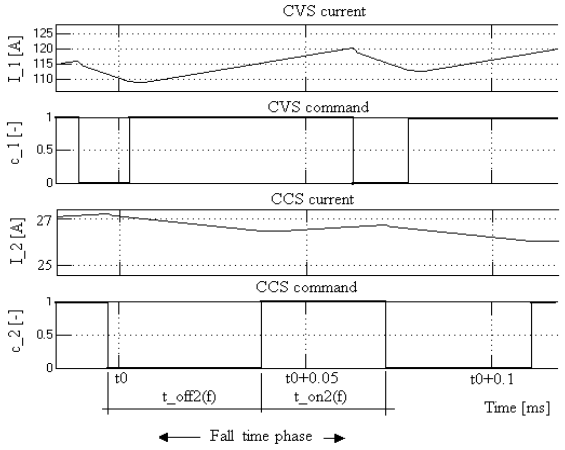


Fig. 7.21b. 6 kW PEMFC case

Fig. 7.21. Zoom of the bi-buck converter behaviour during the mitigation phase [34]

Thus, the average value for the duty cycle of the CCS command is:

$$D_{2r} = \frac{\Delta I_{out(rise)} - n_r T_2 s_6}{n_r T_2 (s_5 - s_6)} \tag{28}$$

In the same manner, during the fall time phase the average value for the duty cycle of the CCS command will be:

$$D_{2f} = \frac{-\Delta I_{out(fall)} - n_f T_2 s_6}{n_f T_2 (s_5 - s_6)} \tag{29}$$

The ratio of the duty cycles, r_D, can be compute as:

$$r_D \overset{\Delta}{=} \frac{D_{2r}}{D_{2f}} \tag{30}$$

Obviously, if the rise time is almost equal to the fall time, then:

$$\Delta t_r \cong \Delta t_f \Rightarrow \begin{cases} \Delta I_{out(rise)} \cong \Delta I_{out(rise)} = \Delta I_{out(ripple)} \\ n_r \cong n_f = n \end{cases} \tag{31}$$

Considering the above data and a switching frequency, f_s, of 10 kHz for both PWM controllers (the buck CVS and the buck CCS controllers), the duty cycle of the switching commands (c1 and c2, respectively) will be:

$$D_1 = \frac{t_{on1}}{T} = \frac{V_{out}}{V_{FC}} \cong 0.75\,, \quad D_2 = \frac{t_{on2}}{T} = \frac{V_{out}}{V_{Bat}} \cong 0.625 \tag{32}$$

The LF to HF current ripple ratio, K_{ripple}, is defined as a ratio betweeen the LF current ripple (peak to peak), $I_{(LF\ ripple)p\text{-}p}$, and the HF current ripple (peak – to - peak), $I_{(HF\ ripple)p\text{-}p}$:

$$K_{ripple} \overset{\Delta}{=} \frac{I_{(LF\,ripple)\,p-p}}{I_{(HF\,ripple)\,p-p}} \cong \frac{f_{(HF\,ripple)}}{f_{(LF\,ripple)}} \tag{33}$$

where $f_{(HF\,ripple)} = f_s$ =10 kHz. Considering the LF power spectrum up to 500 Hz ($f_{(LF\,ripple)}$ =500 Hz), the HF current ripple is more than twenty times lower than the LF current ripple. Taking into account that the PEMFC stack is tolerant to the HF current ripple, it is obvious why the HF current ripple is not considered in the model of load, even if this HF ripple appears (see Fig. 7.12).

When IGBT1 is on (see Fig. 7.17), the second equation (8) can be written as:

$$V_{Bat} = L_2 \frac{\Delta i_2}{t_{on2}} + V_{out} \Rightarrow L_2 \cong \frac{V_{out}(1-D_2)T}{I_{(HF\,ripple)\,p-p}} \tag{34}$$

The value of the buck CCS inductance defines the response time in the tracking loop of the load current shape. Therefore, the mitigation performance for the LF current ripple shown in Fig. 7.5 will be obtained for:

$$L_2 \cong \frac{V_{out}(1-D_2)K_{ripple}}{f_s \cdot I_{(LF\,ripple)\,p-p}} \cong 0.625 \cdot 10^{-3} H \quad (35)$$

As it is known, if the PWM voltage-mode control is used, then the output voltage ripple factor is given by:

$$\frac{\Delta v_{out}}{V_{out}} \cong \frac{\pi^2}{2} \cdot (1 - D_1) \cdot \left(\frac{f_{LC}^*}{f_s} \right)^2, \quad f_{LC}^* = \frac{1}{2\pi\sqrt{LC_f}} \quad (36)$$

If CVS and CCS use the same type of inductor, $L_1 = L_2 = L = 100$ μH, having a series resistance about $r_L = 100$ mΩ, and the RF for the output voltage is set to 4%, then the filter capacitance, C_f, must be greater that 10 μF. A value of 47μF is chosen to assure a ripple factor less than 4%. If a variable-frequency control method will be used, then the switching frequency will be in a range around of 10 kHz. The current ripple amplitude of the filtering capacitors, $i_{Cf(AC)}$, can be estimated using the equation (15):

$$I_{Cf(p-p)} \cong C_f f_s \frac{\Delta v_{out}}{D_1} = C_f f_s V_{FC} \frac{\Delta v_{out}}{V_{out}} \cong 0.6A \quad (37)$$

Consequently, the assumptions that were used to write the above relations have been checked.

If the load current is constant, then an equivalent load resistance can be defined as $R_{out} = V_{out}/I_{out}$. Thus, the associate frequencies are:

$$f_{RC} = \frac{1}{2\pi} \cdot \frac{1}{C_f R_{out}}, \quad f_{RL} = \frac{1}{2\pi} \cdot \frac{R_{out}}{L/2}, \quad f_{LC} = \frac{\omega_n}{2\pi} \quad (38)$$

If the load current is set in the range of the continuous current mode (CCM) operation for the buck CVS, which means $I_{out} < I_{out(base)} \cong 48$ A and $R_{out} > V_{out}/I_{out} \cong 0.5$ Ω, then the associated frequencies will have the same order of magnitude. For example, if $I_{out} \cong 25$ A, then $R_{out} = 1$ Ω, and the associated frequencies are $f_{RC} = 3.3863$ kHz, $f_{RL} = 1.5915$ kHz, and $f_{LC} = 2.3215$ kHz. The same order of magnitude for the associated frequencies of the second-order system means that the system response time is about of $2\pi/\omega_n$, ie 500 μs. The switching period must be lower than the system response time, so the decision to use a 10 kHz switching frequency (or up to this value) represents a good designing option towards applying of the stiff system theory.

7.5 VOLTAGE AND CURRENT-MODE CONTROL TECHNIQUES APPLIED TO FC HPS

7.5.1 Current-mode control

In this section, the simulation results for three types of current-mode control (hysteretic control, PCC, and nonlinear control) for the buck CCS will be presented. Because the first two control methods are classical and easy to be designed, then only the controller structure and the used parameters are shown in the subsections below. Besides those, the systematic design of the nonlinear control law is presented.

7.5.1.1 Hysteretic current-mode control

The structure of the CCS hysteretic controller is shown in Fig. 7.22. The fuel cell base current, $I_{FC(base)}$, is chosen to be close to the MPP value of the FC current, I_{MPP}. The positive ripple of the FC current, $I_{fc(ripple)}$, is quite a lot amplified in the control loop in order to be easy tracked by the CCS current, I_2.

The Ripple Factor for a current type signal, RF_I, is defined as a ratio between the peak-to-peak ripple and its base value:

$$RF_I = \frac{\Delta I_{(ripple)}}{I_{(base)}} \quad (39)$$

Consequently:

$$RF_{out} = \frac{\Delta I_{out(ripple)}}{I_{out(base)}} \quad (40)$$

$$RF_{FC} = \frac{\Delta I_{FC(ripple)}}{I_{FC(base)}} \quad (41)$$

So, considering the relationships (41) and (42), the mitigation loop gain, G_{Ifc}, must be established in accordance:

$$G_{I\,fc} = \frac{\Delta I_{CCS(ripple)}}{\Delta I_{FC(ripple)}} \cong \frac{\Delta I_{out(ripple)}}{\Delta I_{FC(ripple)}} \cong \frac{RF_{out}}{RF_{FC}} \cdot \frac{\eta_1 V_{FC(base)}}{V_{out}} \Rightarrow G_{I\,fc} \cong \frac{RF_{out}}{RF_{FC}} \cdot G_{1(base)} \tag{42}$$

Thus, considering the imposed value of RF_{FC}, the mitigation loop gain, G_{Ifc}, can be designed based on the know value of the RF_{out}. For example, if $I_{fc(ripple)p\text{-}p} \cong 10\%\ I_{MPP}$ is chose, then the base operating point ($I_{FC(base)}$, $V_{FC(base)}$) is about (40 A, 33 V) and (108 A, 55 V) for the 1,26 kW and 6 kW HPS, respectively. Using the simulation results performed and shown above for G_{Ifc}=100, the RF and G^*_{Ifc} values can be computed for the 1,26 kW PEMFC stack, as below:

$$\left.\begin{aligned} RF_{out} &\cong \frac{95-50}{50} = 90\% \\ RF_{FC} &\cong \frac{43.38-42.9}{42.9} \cong 1.1\% \end{aligned}\right\} \Rightarrow G^*_{I\,fc} \cong \frac{90}{1.1} \cdot \frac{0.9 \cdot 33}{25} \cong 95.5 \tag{43}$$

The RF and G^*_{Ifc} values for the 6 kW PEMFC stack and G_{Ifc}=100 are:

$$\left.\begin{aligned} RF_{out} &\cong \frac{240-120}{120} \cong 92\% \\ RF_{FC} &\cong \frac{95.5-91.5}{91.5} \cong 4.4\% \end{aligned}\right\} \Rightarrow G^*_{I\,fc} \cong \frac{92}{4.4} \cdot \frac{0.9 \cdot 55}{40} \cong 25.9 \tag{44}$$

Also, the simulation results for the 1.26 kW PEMFC stack and G_{Ifc} = 80 are shown in Fig. 7.23. In this case, the G^*_{Ifc} gain is computed:

$$\left.\begin{aligned} RF_{out} &\cong \frac{95-50}{50} = 90\% \\ RF_{FC} &\cong \frac{43.85-43.1}{43.1} \cong 1.74\% \end{aligned}\right\} \Rightarrow G^*_{I\,fc} \cong \frac{90}{1.74} \cdot \frac{0.9 \cdot 33}{25} \cong 61 \tag{45}$$

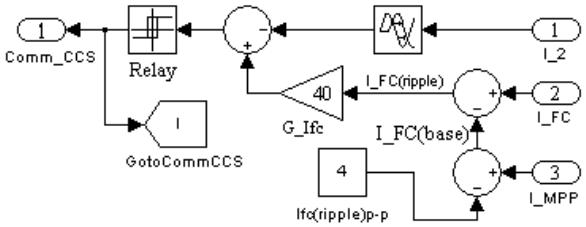


Fig. 7.22. The structure of the CCS hysteretic controller [34]

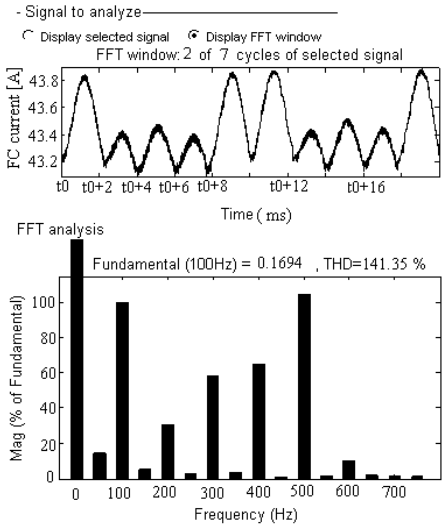


Fig. 7.23. The FC current (top) and its power spectrum (bottom):
1.26 kW HPS case, having the CCS Hysteretic controller with G_{Ifc}=80 [34]

From these results it can be concluded that between the set gain (G_{Ifc}) and the computed gain (G^*_{Ifc}) there is a nonlinear relation of dependence. This non-linear law will be analyzed in the subsection dedicated to the nonlinear control.

7.5.1.2 Peak current-mode control

The structure of the CCS PCC controller is shown in Fig. 7.24. The buck converter will operate at the switching frequency of 10 kHz set by the pulse generator.

The simulation results are shown in Fig. 7.25 for the 1.26 kW HPS using G_{Ifc} = 80. It can be observed that the mitigation performances are almost the same for both hysteretic and PCC controllers (see Fig. 7.23 and 7.25).

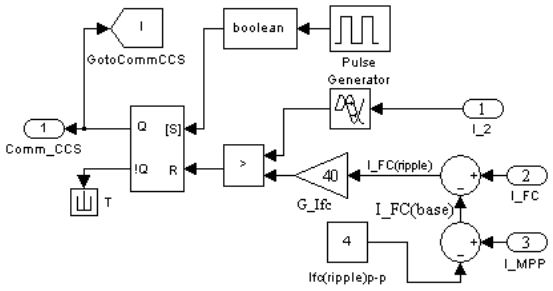


Fig. 7.24. The structure of the CCS PCC controller [34]

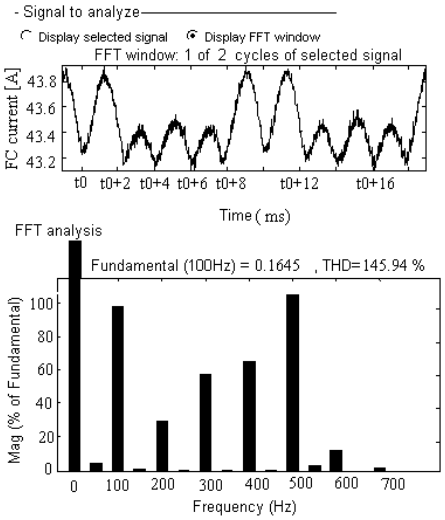


Fig. 7.25. The FC current (top) and its power spectrum (bottom): 1.26 kW HPS case, having the CCS PCC controller with G_{Ifc}=80 [34]

The output voltage is shown in Fig. 7.26. The power spectrum is spread in the LF band based on the anti-control technique implemented in the CVS controller, which will be explained later in this chapter. Note that the switching frequency harmonics can still be seen, thus this kind of control could be further improved.

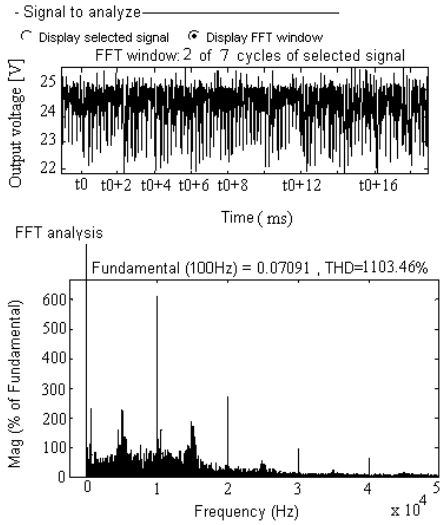


Fig. 7.26. The output voltage (top) and its power spectrum (bottom): 1.26 kW HPS case, having the CCS PCC controller with G_{Ifc}=80 [34]

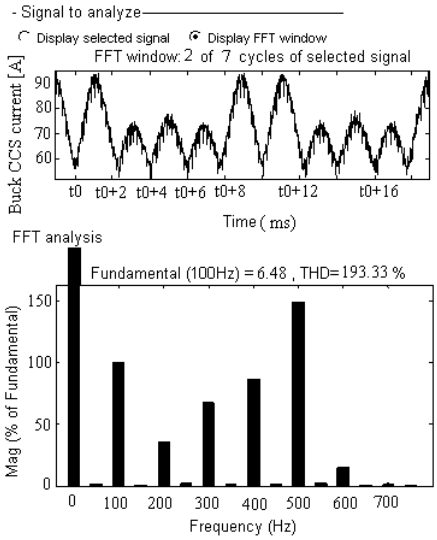


Fig. 7.27. The buck CCS current (top) and its power spectrum (bottom): 1.26 kW HPS case, having the CCS PCC controller with G_{Ifc}=80 [34]

Taking into account that the spectrum of the FC current is almost the same for the both CCS controllers (see Fig. 7.23 and 7.25), it is obvious that the buck CCS current spectrum will be almost the same, too (see Fig. 7.27). Because the FC ripple is much smaller than the load ripple, it is can be observed that the magnitudes of the fundamental frequency for the buck CCS current and the load current are almost equal (see Fig. 7.5 and 7.27). Obviously, the magnitudes difference will be propagated back to the PEMFC stack (see Fig. 7.25).

The same results are obtained for the 6 kW HPS using both CCS controllers.

7.5.1.3 Nonlinear current-mode control

In the previous two sections it was shown that the mitigation performance of the FC current ripple depends on G_{Ifc} gain. Using simulation for a 1.26 kW HPS that uses a CCS hysteretic controller, the characteristics of the FC current ripple vs. the set G_{Ifc} gain and the FC harmonic magnitude vs. the set G_{Ifc} gain can be drawn (see Fig. 7.28). It can be observed that almost the same shape as in Fig. 7.13.a is obtained. Thus, the mitigation ripple based on CCS gives almost the same FC ripple whatever level power is. The characteristic of the computed gain (G^*_{Ifc}) vs. the set gain (G_{Ifc}) is shown in Fig. 7.29. These characteristics were drawn in the same manner used for the 6 kW HPS case study. These characteristics also show that the G_{Ifc} gain must be nonlinear in order to obtain the same FC ripple factor for different load ripple. So, the CCS controller must have both ripples as input variable. The design of the CSS controller will be shown in the next subsection based on the FLC controller.

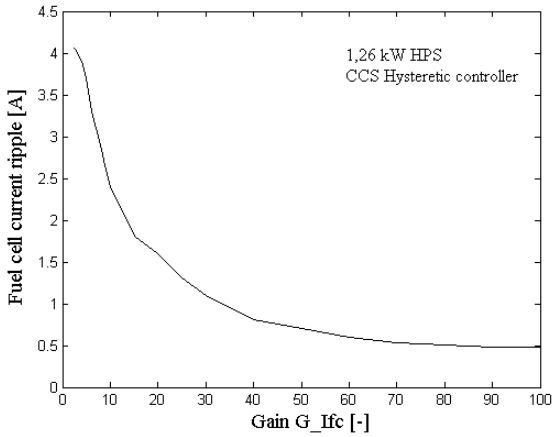


Fig. 7.28. The FC current ripple vs. G_{Ifc} gain set [34]

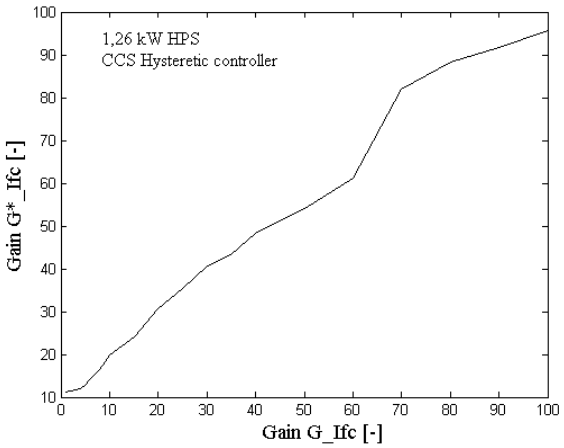


Fig. 7.29. The computed gain G^*_{Ifc} vs. G_{Ifc} gain set [34]

7.5.1.4 Designing of the nonlinear control law

An accurate model of the HPS system is too complex due to the nonlinearities that are included in all models of the HPS subsystems. Consequently, the nonlinear control law will be designed based on FLC.

First of all, the input variables are defined as it was mentioned above. Obviously, the first input is the FC current ripple. The second variable was chosen to be the CCS current ripple. This signal tries to track the load ripple, so it is a measure of it, too. The CCS current is generated via the buck CCS as an anti-ripple of the inverter ripple, which is the HPS output ripple ($I_{inverter(ripple)} \cong I_{load(ripple)}$). Thus, this is also a measure of it ($I_{2(ripple)} \cong I_{load(ripple)}$). Compared to the CCS current ripple, the inverter ripple has HF components with high magni-

tudes (see Fig. 7.12) that could perturb the tracking loop. If a low-pass filter will be used to obtain the LF profile of the inverter ripple, then a variable phase shift will appear between the input variables. Consequently, the CCS current ripple is better to be considered as a second variable, to overcome these problems (see Fig. 7.30).

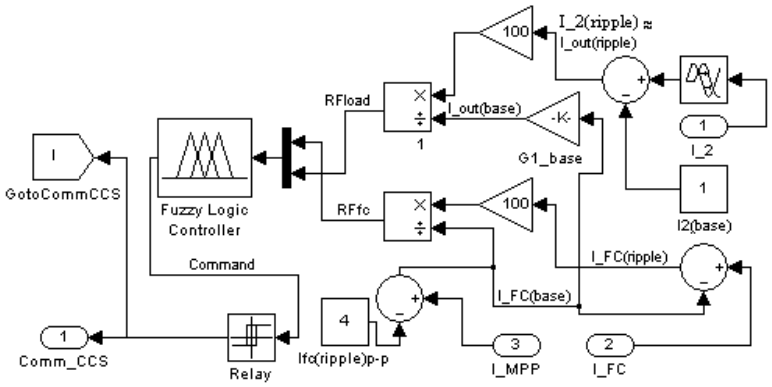


Fig. 7.30. The structure of the CCS FLC controller [34]

Also, the input variables were normalized, considering their ripple factors (noted as RF_{fc} and RF_{load}). The membership functions for both input variables, RF_{fc} and RF_{load}, are shown in Fig. 7.31. Four membership's functions are defined for both input variables in correlation with the design goal. They are named as VS=Very Small, S=Small, B=Big and VB=Very Big (see Fig. 7.31). Also, five membership functions are uniformly defined for the output variable, named the CCS command signal (com). They are named as VS=Very Small, S=Small, N=Nominal, B=Big and VB=Very Big.

The rules base is shown in Table 7.4.

Table 7.4. The FLC rules base [34]

Command signal		RFfc			
		VSfc	Sfc	Bfc	VBfc
RFload	VSrm	Ncom	Scom	VScom	VScom
	Srm	Bcom	Ncom	Scom	VScom
	Brm	VBcom	Bcom	Ncom	Scom
	VBrm	VBcom	VBcom	Bcom	Ncom

The Mamdani implication and the centre of gravity defuzzification method are used. The desired control surface is obtained through the position of the membership functions for the input variables (see Fig. 7.32). The contours projected for different levels of the CCS command signal are shown in Fig.7.33.

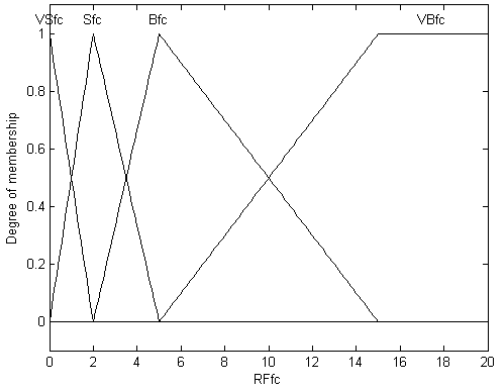


Fig. 7.31.a. Membership functions for the FC ripple factor

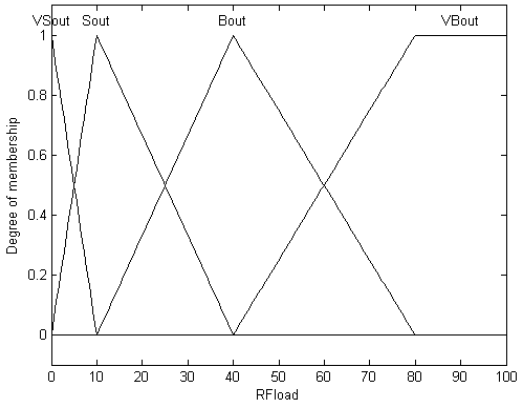


Fig. 7.31.b. Membership functions for the load ripple factor

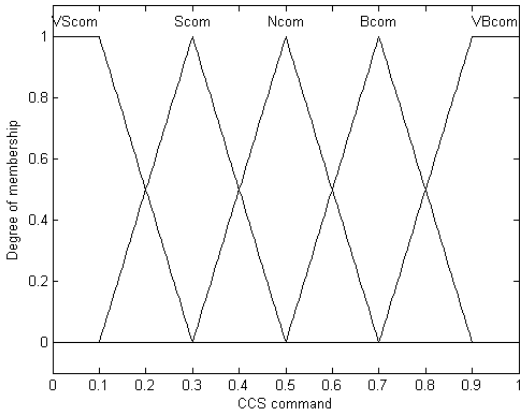


Fig. 7.31.c. Membership functions for the CCS command signal

Fig. 7.31. The membership functions for the FLC variables [34]

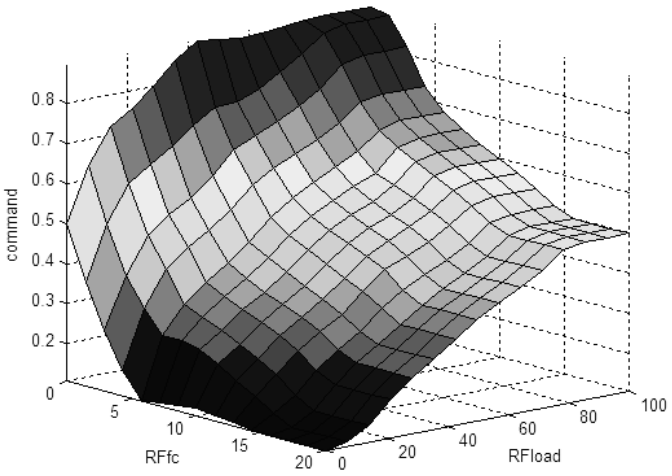


Fig. 7.32. The FLC control surface [34]

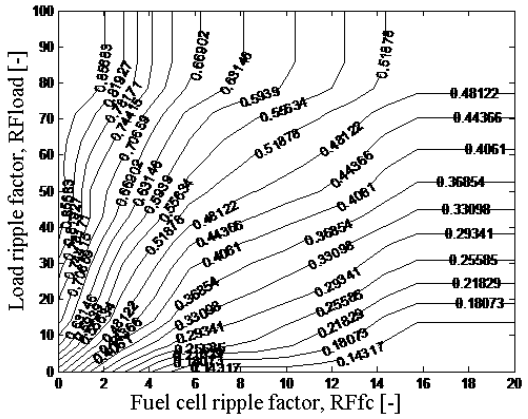


Fig. 7.33. The projected contours for the FLC control surface [34]

The base reference for different currents is defined to have a positive ripple. The base reference for the CCS current, $I_{2(base)}$, was set close to zero (1 A) to reduce the size of the battery that supplies the buck CCS converter. The battery will be designed to meet the load ripple and some transient peaks of power. The base reference for the FC current, $I_{FC(base)}$, was chosen close to the MPP ($I_{FC(base)}$=$I_{FC(base)}$ - $I_{fc(ripple)p\text{-}p}$) to increase the energy efficiency of the FC stack. The FC ripple, $I_{fc(ripple)p\text{-}p}$, was set to 4 A, up to the value that it is obtained without the use of the buck CCS converter (setting G_{Ifc} = 0 in the tracking loop; see Fig. 7.28). The base reference for the load current, $I_{out(base)}$, is computed using the $G_{1(base)}$ gain:

$$G_{1(base)} \overset{\Delta}{=} \frac{\eta_1 V_{FC(base)}}{V_{out}} \cong \frac{I_{out(base)}}{I_{FC(base)}} \qquad (46)$$

If the relay block has the on/off switching levels at 0.45 and 0.5 (0.475±0.025), then the nonlinear characteristic of the RF_{fc} vs. RF_{load} obtained for the 0.475 command level (see Fig. 7.33) can be considered in the design of the transfer characteristic: the equivalent load RF ($EqRF_{load}$) vs. RF_{fc} (see Fig. 7.34). This nonlinear control law of $EqRF_{load}$ vs. RF_{fc} can be also obtained directly using a single-input single–output (SISO) FLC. The designing of the SISO FLC is given below.

The input variable, RFfc, and the output variable, EqRFload, have the same membership functions defined as in Fig. 7.31. The rules base is shown in Table 7.5. The Mamdani implication and the centre of gravity defuzzification method are used. The FLC control surface obtained is shown in Fig. 7.27.

Table 7.5. The SISO FLC rules base [34]

	RFfc

	VSfc	Sfc	Bfc	VBfc
EqR-Fload	Vsload	Sload	Bload	VBload

Obviously, this characteristic is close to one of the projected contours shown in Fig. 7.33, namely the one that is obtained for the level of command signal set to approximately 0.48. Thus, the structure of the CCS FLC controller is redesigned as in Fig. 7.35 based on this nonlinear control law shown in Fig. 7.34. The nonlinear control law can be simply implemented based on a PWL nonlinear gain. For example, the PWL nonlinear gain having the input vector [0, 4, 16, 20] and the output vector [0, 40, 80, 80]) is easy to be implemented.

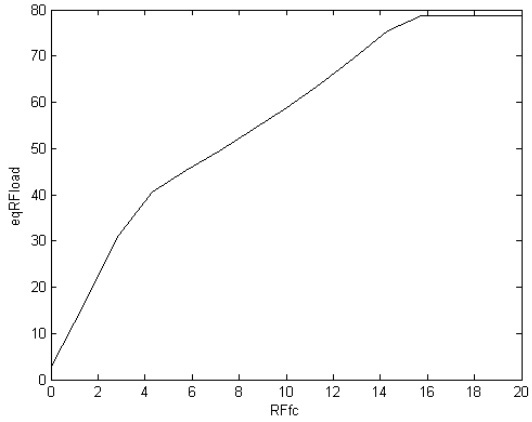


Fig. 7.34. The nonlinear control law of the EqRFload vs. RFfc [34]

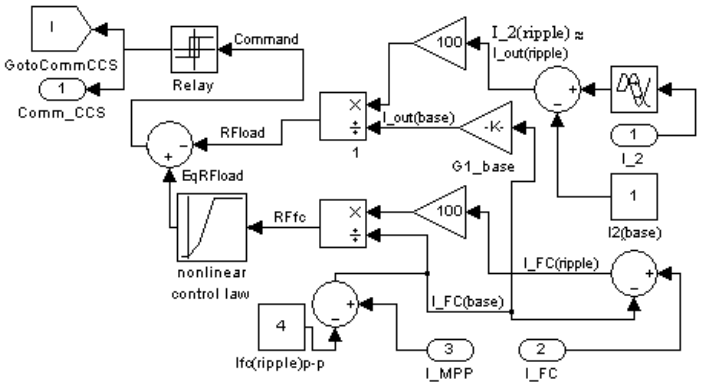


Fig. 7.35. The structure of the CCS nonlinear controller [34]

7.5.1.5 Simulation results

The start-up of the mitigation process is almost the same as in the case of the FC HPS that uses the CCS hysteretic controller (see Fig. 7.18). The simulation results for the 1.26 kW HPS, which uses the PWL nonlinear controller proposed, are shown in Fig. 7.36. It can be observed that the mitigation performances are better compared to the use of the hysteretic or PCC controller (to compare, see Fig. 7.23 and 7.25). For example, the 100 Hz harmonics have a magnitude of approximately 0.074 (using PWL nonlinear controller) instead of approximately 0.17 (using hysteretic controller). Thus, the magnitude of 100 Hz harmonic is about two times smaller (0.074/0.17≅1/2).

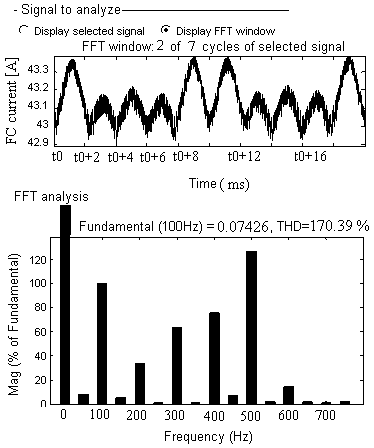


Fig. 7.36. The FC current (top) and its LF power spectrum (bottom): 1.26 kW HPS case with the CCS PWL nonlinear controller [34]

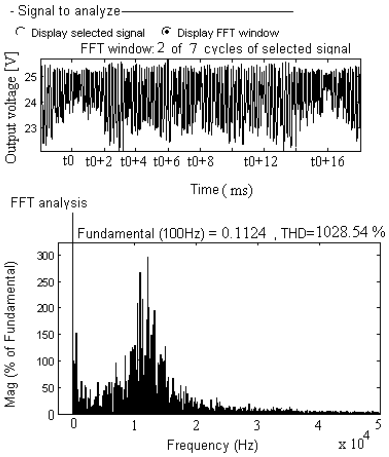


Fig. 7.37. The output voltage (top) and its power spectrum (bottom): 1.26 kW HPS case with CCS PWL nonlinear controller [34]

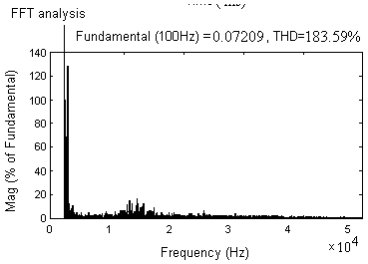


Fig. 7.38. The HF power spectrum of the FC current:
1.26 kW HPS case with CCS PWL nonlinear controller [34]

The output voltage and its power spectrum are shown in Fig. 7.37 for a 1.26 kW HPS that uses the PWL nonlinear controller. The power spectrum was spread in the HF band up to 20 kHz. This HF ripple also appears in the power spectrum of the FC current (see Fig. 7.38), but it is much smaller than the LF ripple, being up to the allowable limits. Consequently, it is well tolerated by the PEMFC stack. The main advantage of the PWL nonlinear controller is its design that is not dependent to the level of HPS power. The simulation results for a 6 kW HPS are shown in Fig. 7.39 and 7.40 to prove this advantages. So, using the simulation results shown in Fig. 7.39 and 7.40, the RF and GIfc values can be computed as below:

$$\left.\begin{aligned} RF_{out} &\cong \frac{188-110}{110} = 71\% \\ RF_{FC} &\cong \frac{91-89.7}{89.7} \cong 1.4\% \end{aligned}\right\} \Rightarrow G_{Ifc}^{*} \cong \frac{90}{1.1} \cdot \frac{0.9 \cdot 61}{40} \cong 70 \tag{47}$$

It can be observed that the RF of the FC current, RF_{FC}, has now almost the same value (1.1% and 1.4%) for the both HPS power levels, not four times higher (see relationships 43, 44 and 47).

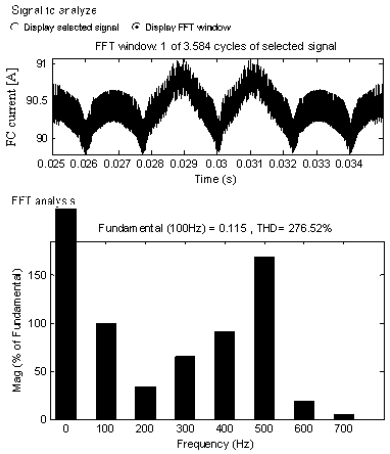


Fig. 7.39. The FC current (top) and its LF power spectrum (bottom): 6 kW HPS case with CCS PWL nonlinear controller [34]

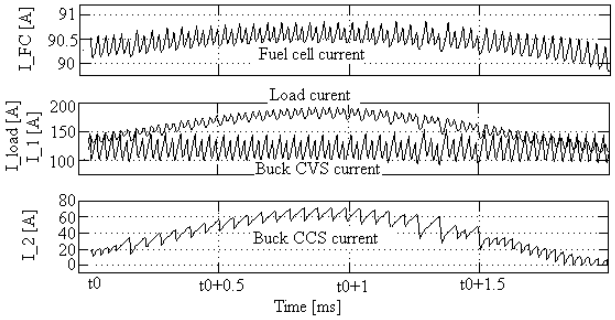


Fig. 7.40. The behaviour of the 6 kW HPS case with CCS PWL nonlinear controller [34]

The case of a three-phase inverter system powered by a 20 kW HPS (see Fig. 7.16.a) is analyzed in order to show that the proposed PWL nonlinear controller will operate almost as well if an inverter system is used instead of the equivalent load. The current and the voltage of the 20 kW PEMFC stack are approximately 45 A and 435 V, close to the MPP. The reference voltage of the buck CVS is set to 400 V.

The simulation results for the FC current and voltage are shown in Fig. 7.41 and 7.42 considering the bi-buck topology for the FC HPS (Fig. 7.17). The RF of the FC current is about of 0.8%. The RF of the HPS output voltage is approximately 3.5% and 0.3% using a C_f filter capacitance of 470 μF and 4700 μF, respectively (see Fig. 7.43).

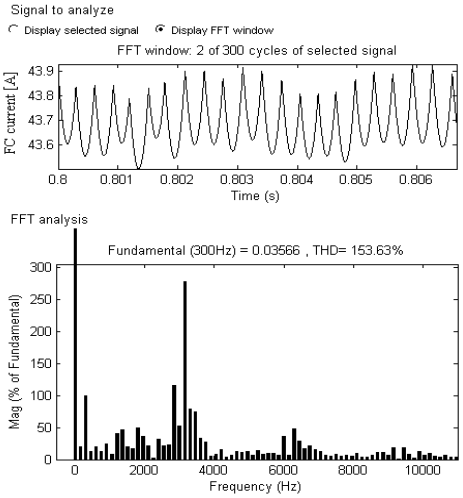


Fig. 7.41. The FC current (top) and its power spectrum (bottom) for the 20 kW HPS case [34]

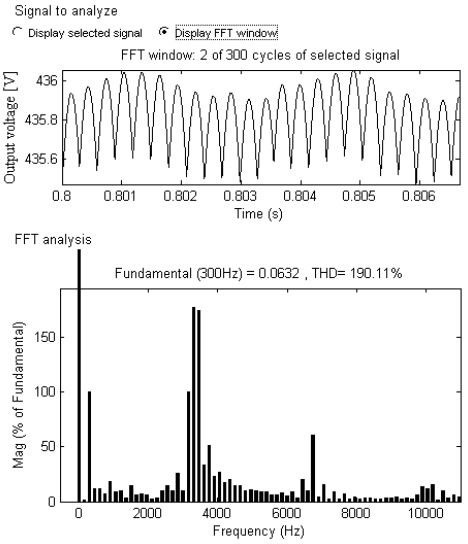
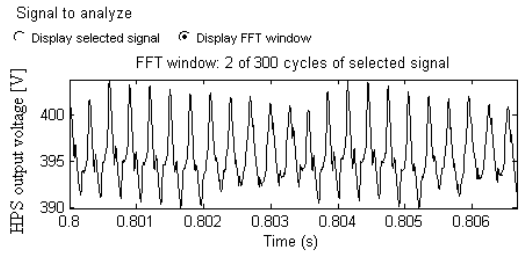


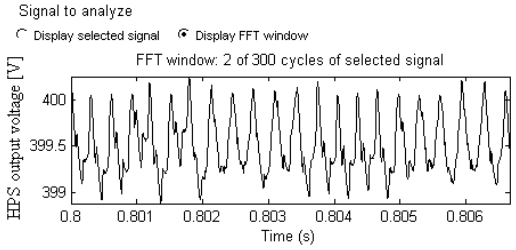
Fig. 7.42. The FC voltage (top) and its power spectrum (bottom) for the 20 kW HPS case [34]

The three-phase inverter system structure is a full-bridge that uses a switching command of pure sine PWM type (having the carrier frequency set to 10 kHz). A classic voltage control of the AC output voltage is used.

The input current and its power spectrum are shown in Fig. 7.44. This current has LF harmonics (see middle plot of Fig. 7.44) and, for example, the magnitude of the 300 Hz fundamental harmonic is 1.886 A. This LF current ripple will be mitigated by the injection of an anti-ripple current via the buck CCS. The buck CCS current and its power spectrum are shown in Fig. 7.45.



a) C_f=470 μF



b) C_f=4700 μF

Fig. 7.43. The HPS output voltage for the 20 kW HPS case [34]

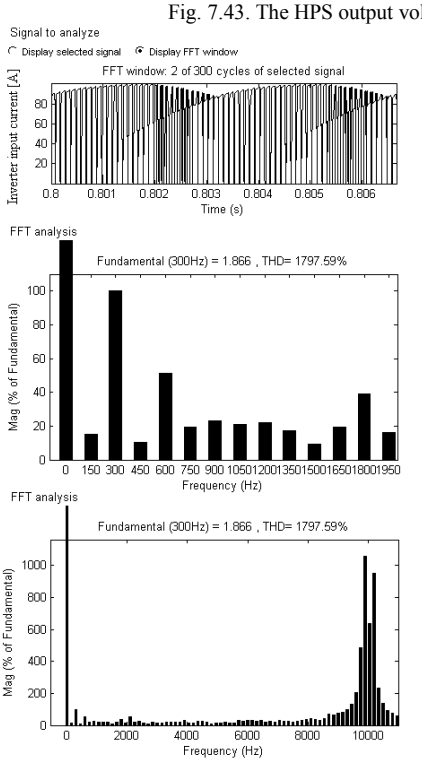


Fig. 7.44. The input current of the three-phase inverter system [34]

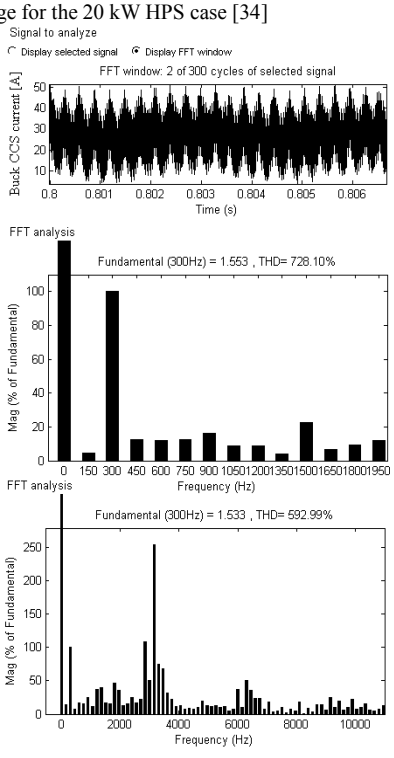


Fig. 7.45. The buck CCS current [34]

It can be observed that the magnitude of the 300 Hz fundamental harmonic is 1.553 A. The difference between those currents (0.333 A) is the output current of the CVS (see Fig. 7.40) and this current ripple is back propagated to the PEMFC stack. The 300 Hz fundamental magnitude of the PEMFC current is 0.03566 A (see Fig. 7.41). The mitigation ratio for the fundamental harmonic of the inverter ripple is approximately 1.8 %. Also, the mitigation of the fundamental harmonic based on the use of the buck CVS is about nine times (0.333/0.03566≅9.34)

It can be observed that the LF shape of the buck CCS current (top plot of Fig. 7.45) tracks the LF shape of the input inverter current (top plot of Fig. 7.44). This is because the buck CVS mitigates the LF harmonics in the same ratio, which is about 9. The power spectrum of the HPS signals, which is shown in Fig. 7.41, 7.42 and 7.45, reveals that this is spread in a large band.

This section analyzes the bi-buck topology as a solution to mitigate the inverter ripple. The simulation results have shown that the mitigation performance depends on the magnitude of the ripple and on the level of the load power. Consequently, a nonlinear controller for the buck CCS is necessary to be designed in order to overcome these issues. The RF for the inverter ripple is up to 3%, that is reported in [43].

The nonlinear controller for the buck CVS will be presented in next section.

7.5.2 Voltage-mode control

The nonlinear control law of the CVS controller will be designed based on a SISO FLC.

7.5.2.1 Designing of the nonlinear voltage controller

Note that the buck CVS converter is the power interface of the FC stack (see Fig. 7.16) and the CVS controller structure is shown in Fig. 7.46.

The rules base used to obtain a nonlinear characteristic to mitigate the output voltage ripple is very simple: (1) if the output voltage ripple is small, then the loop gain must be small; (2) if the output voltage ripple increases, then the loop gain must rise quickly; (3) if the output voltage ripple is high, then the loop gain must be limited to a value that ensures the stability of the overall feedback loop. The main design questions are related to how small must be, how quickly must increase and how big should be the limit of the loop gain. The fuzzy logic reasoning based on systematic approach will be used to design the CVS nonlinear control law. The CVS controller is a single input – single output system. The input is the output voltage error, v_{error}, and the output is the v_2 voltage, having values in range of [-1V, 1V] and [-10V, 10V], respectively.

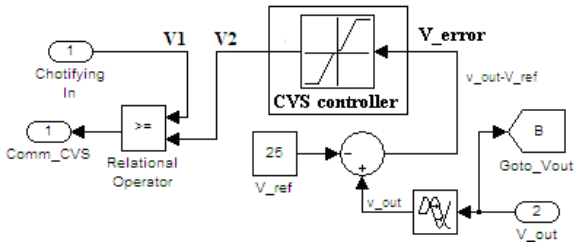


Fig. 7.46. The CVS controller that implement the voltage-mode nonlinear control proposed [33]

The v_2 voltage range must be correlated with the range of the chaotifying signal, which can be any periodic signal. The saw-tooth signal, $v_1(t)$, will be used in this section as a chaotifying signal:

$$v_1(t) = V_L + (V_H - V_L)\frac{t(\mathrm{mod}\, T_{sw})}{T_{sw}} \tag{45}$$

This is a ramp voltage that decreases in a time period, $T_{sw}=1/f_{sw}$, from a higher voltage, V_H , to a lower voltage, V_L. The values used in all simulations are V_H = 9 V, V_L = 1 V, and f_{sw}=10 kHz. These were chosen as in [41] in order to compare the obtained results.

The output voltage is set to 25V, so a RF of 4% means an output voltage error of 1V. Consequently, the range of the output voltage error was chosen to be [-1V, 1V]. The CVS controller was replaced with a proportional controller. Through the trial and the error method a gain of 10 for which the RF is of 4% was found. So, the range [-10V, 10V] was chosen for the V_2 voltage. Thus, for the output voltage error, seven membership functions are symmetrically defined in these ranges (see Fig. 7.47: Very_Big_Negative (VBN), Big_Negative (VBN), Negative (N), Zero_Equal (ZE), Positive (P), Big_Positive (BP), and Very_Big_ Positive (VBP)) and V_2 voltage (see Fig. 7.48: Very_Very_Small (VVS), Very_Small (VS), Small (S), Zero (Z), Big (B), Very_Big (VB), and Very_Very_Big (VVB)). Taking in account the basic idea to obtain the nonlinear characteristic of the CVS controller, the base of rules is shown in Table 7.6:

Table 7.6. The rules base for CVS fuzzy controller [33]

Rule	Output voltage error	Output voltage of the CVS controller
1	VBN	VVS
2	BN	VS
3	N	S
4	ZE	Z
5	P	B
6	VP	VB
7	VBP	VVB

The control law is obtained by defining the position of the peaks for the membership functions. The Z and ZE triangular membership functions have the peak set to zero. The rest of the triangular membership functions for the output voltage error have the peaks set to ±50 mV, ±250 mV, and ±1000 mV, which means a RF of 0.2%, 1%, and 4%, respectively.

The triangular membership functions for the V_2 voltage (namely the B and VB, and their symmetrical membership functions, S and VS, respectively) have the peaks to ±100mV and ±500mV in order to result the same gain (100mV/50mV=500mV/250mV=2).

The VVS and VVB trapezoidal memberships are defined (as ±0.5, ±1, ±10, ±10) to result an output voltage ripple factor up to 4%. The peaks of the VBN and VBP triangular membership functions were set to ±1V in order to have a small gain at ±1V output voltage error (equal with 1V/1V=1) and a high gain at ±10V output voltage error (equal with 10V/1V=10).

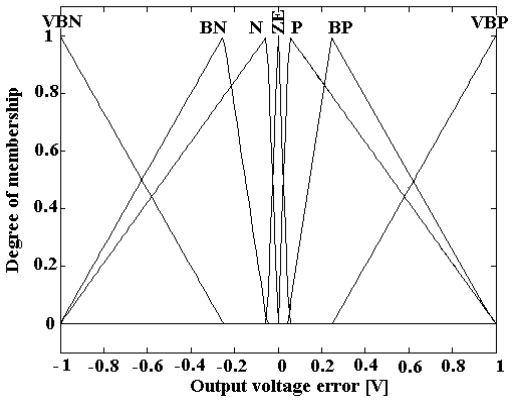


Fig. 7.47. The membership functions for the output voltage error [33]

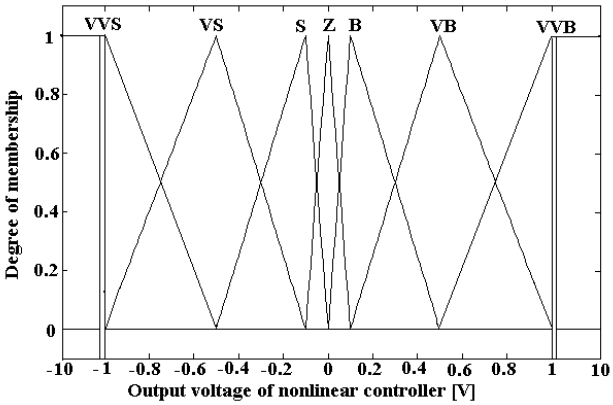


Fig. 7.48. The membership functions for the output voltage the of nonlinear voltage-mode controller [33]

The obtained nonlinear voltage-mode control law is shown in Fig. 7.49. Note that the Mamdani implication, max-min fuzzy connectives and the centre of the area defuzzification strategy were used. The PWL voltage-mode control law that fit the nonlinear voltage-mode control law is also shown in Fig. 7.49.

The PWL voltage-mode control law can be easily implemented by the following look-up table [42]:

- input vector: [-1, -0.5,-0.15, 0.15, 0.5, 1];
- output vector: [-10,-10,-0.4, 0.4, 10, 10].

A mathematical approach of the buck CVS in a closed control loop can be performed based on this PWL voltage-mode control law [32]. The saw-tooth signal operates as a chaotifying signal (see Fig. 7.50). It is observed that output voltage of the nonlinear controller is a distorted signal, obtained from the output voltage error via the PWL voltage-mode control law.

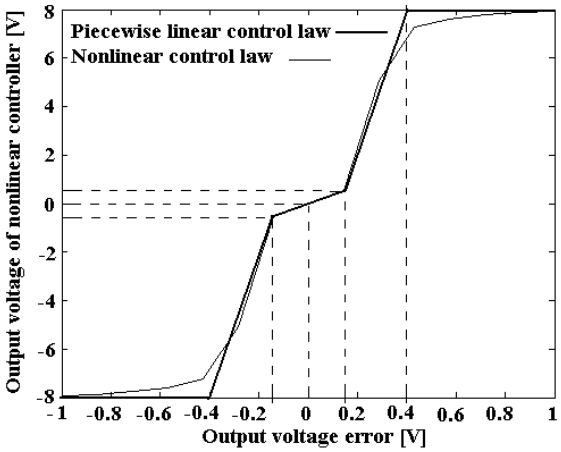


Fig. 7.49. The nonlinear voltage control characteristic (thin line) and PWL voltage control characteristic (thick line) which is fitted on it [33]

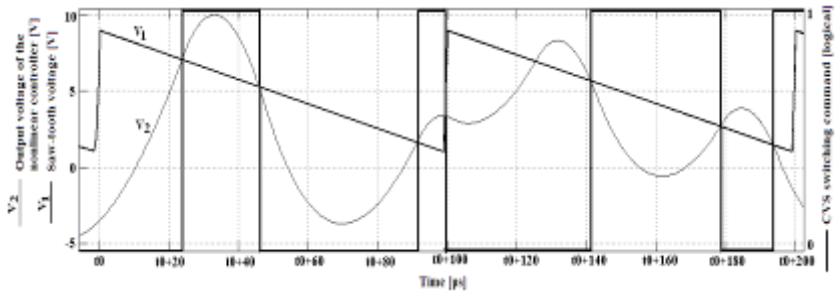


Fig. 7.50. Signals related to CVS controller operation with saw-tooth as chaotifying signal [33]

The performance of the output voltage regulation for the CVS controller is evaluated for different load currents (see Fig. 7.51). It can be seen that the output voltage is well regulated to the reference voltage of 25 V. The PEMFC time constant was set to 0.2 s.

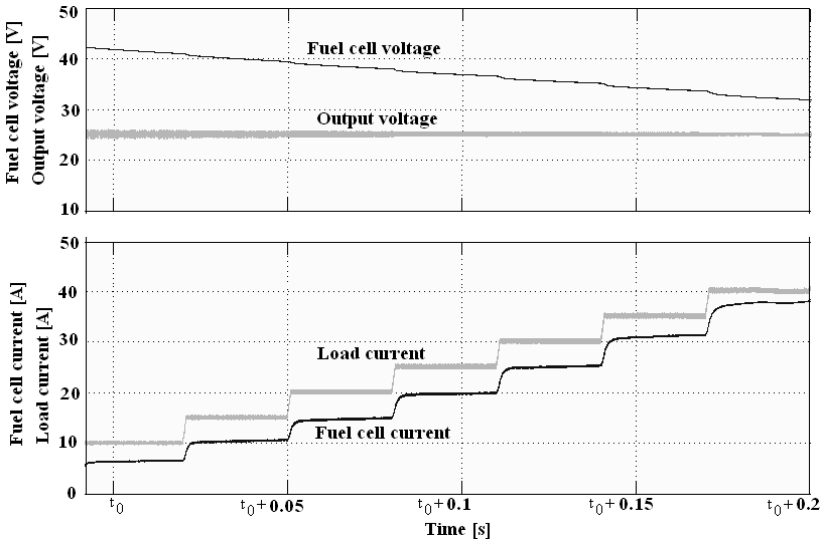


Fig. 7.51. The behaviour of the CVS controller tested with step-up load current [33]

7.5.2.2 Simulation results

Two performance indicators, PI_1 and PI_2, are used to quantify the spreading level of the output power [32, 42]:

$$PI_1 = \frac{\Delta f_{10\%}}{f_{COG}}, \quad PI_2 = \frac{S_{peak}}{THD} \tag{46}$$

where:

S_{peak} is the maximum spectral magnitude (as % of DC component), excluding the harmonics of the chaotifying signal that can possibly occur (see Fig. 7.52);

$\Delta f_{10\%Sp}$ - the frequencies band where the magnitude of the power spectrum is 10% over the S_{peak};

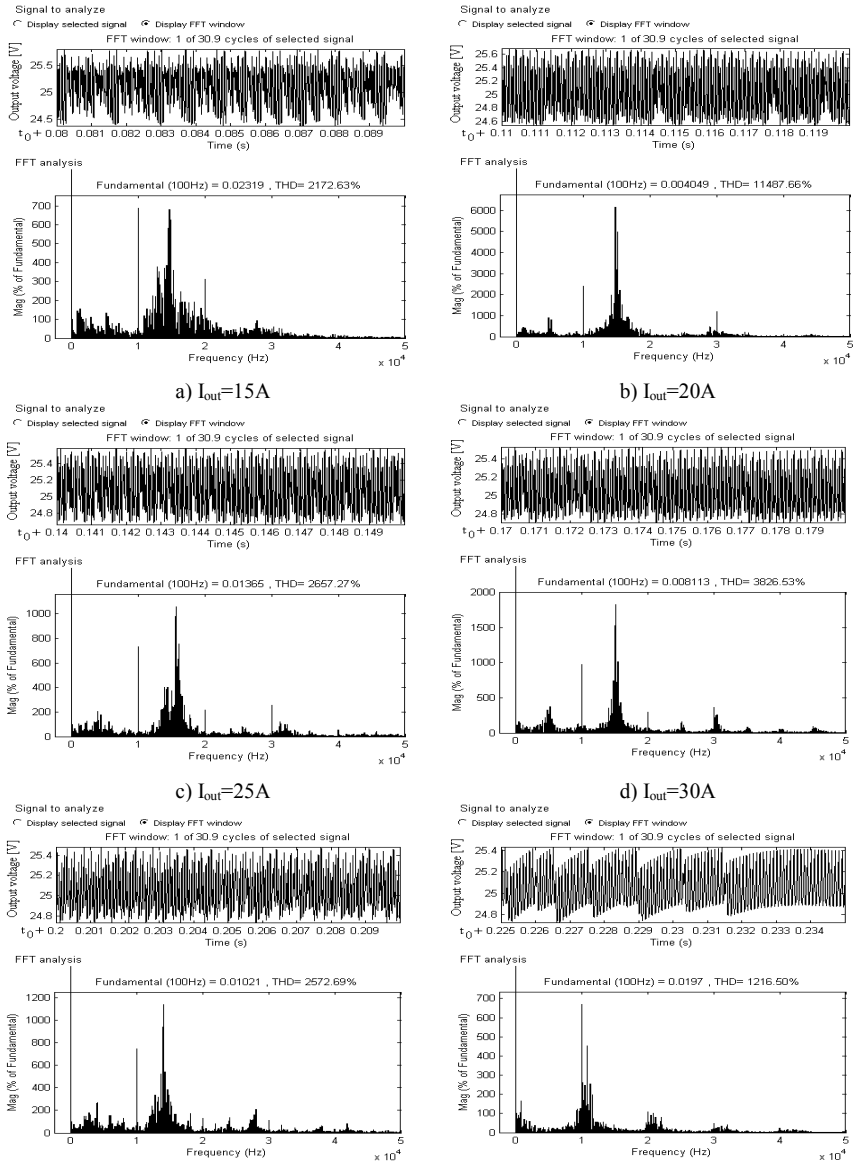
f_{COG} - the frequency that is the centre-of-gravity of the power spectrum;

THD – the total harmonic distortion factor of the output voltage.

For example, the performance indicators could be interpreted as below:

- If PI_1 >50%, then $\Delta f_{10\%Sp} > f_{COG}/2$, and this means a large frequencies band where the most part of the spread power spectrum is situated;

- If PI_2 <50%, then S_{peak} <THD/2, and this means no high peak in the power spectrum.



a) I_{out}=15A b) I_{out}=20A

c) I_{out}=25A d) I_{out}=30A

e) I_{out}=35A f) I_{out}=40A

Fig. 7.52. The output voltage (top) and its power spectrum (bottom) for different load current, using the simulation parameters: f_{sw}=10 kHz, L=100μH, and C=47μF [33]

The performance indicators are estimated for different load currents (see Fig. 7.52). Thus, the performance indicators are about PI_1≅27 kHz / 18 kHz≅150% and PI_2≅1400/6183≅23%, and PI_1 ≅11 kHz / 17 kHz≅105% and PI_2 ≅2200/8000≅28%, for simulation results shown in Fig. 7.53 and 7.54, respec-

tively. So, a well spreading performance is obtained in both cases. Note that the harmonics of the chaotifying signal occur in last case and all simulations shown in Fig. 7.51. This situation can be avoided by pseudo-randomize of the saw-tooth period. The output voltage ripple factor, $RF_{Vout}=\Delta v_{out}/V_{out}$, is approximately 0.24% and 2.4%, respectively.

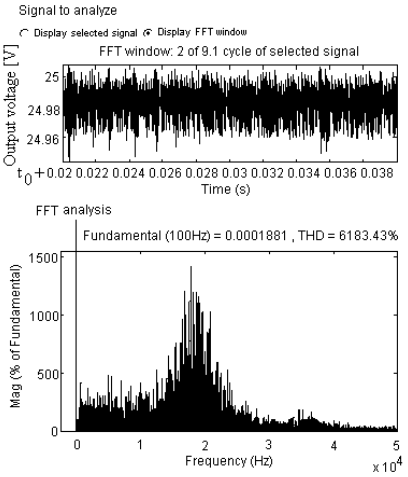


Fig. 7.53. The output voltage (top) and its power spectrum (bottom) with the parameters [33]: f_{sw}=15 kHz, L=100 μH, C=47 μF, R_{out}=1 Ω

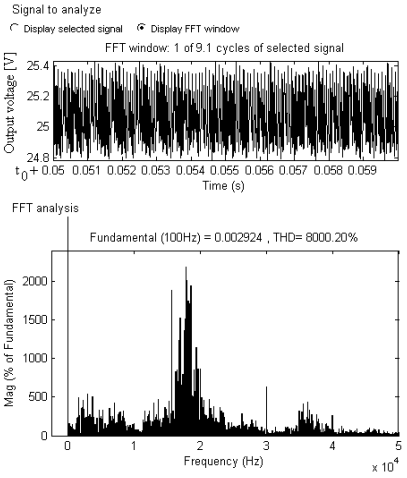


Fig. 7.54. The output voltage (top) and its power spectrum (bottom) with the parameters [33]: f_{sw}=15 kHz, L=100 μH, C=47 μF, R_{out}=2/3 Ω

The performance indicators PI_2, PI_1 and RF_{Vout} are estimated in Table 7.7, for the case study shown in Fig. 7.52. Note that the level of the load current influences the performance indicators by changing the associated frequencies of the buck CVS converter (f_{RL} and f_{RC}).

Table 7.7. The performance indicators for the case study shown in Fig. 7.52 [33]

I_{out} [A]	f_{RL} [kHz]	f_{RC} [kHz]	PI_1 [%]	PI_2 [%]	RF_{Vout} [%]
15	2.6526	2.0318	79	32	5.6
20	1.9894	2.7090	42	52	4
25	1.5915	3.3863	35	41	3.2
30	1.3263	4.0635	25	47	3.2
35	1.1368	4.7408	34	46	3.2
40	0.9947	5.4180	27	55	3.2

If the buck parameters are L=100 μH and C=47 μF, then the natural frequency, f_{LC}, will be 2.3215 kHz. So, looking into Table 7.7 and also taking in account other simulation results, it can be concluded that a well spreading level of the power spectrum could be obtained if the associated frequencies have the same order of magnitude. The output voltage ripple factor is up to 4% for the

load current in the rated range. The response in the output voltage is lower than the voltage ripple if a 5 A step-up in the load current is used (Fig. 7.51). These results have shown the control robustness of the CVS controller. If a load current pulse over 10 A is used, then small voltage spikes appear on the output voltage during the rise and fall time of the load current pulse (Fig. 7.55). These spikes can be better compensated using a higher value for the filtering capacitor on the DC bus or via the buck CCS.

The resistive parameter of the load pulse, Rout(pulse), is 2/3Ω from 40ms to 80ms and 1Ω in rest. Thus, the load current pulse is 12.5 A, and the FC current pulse can be estimated by (47):

$$I_{FC(pulse)} \cong \frac{V_{out}}{\eta_1 V_{FC(pulse)}} \cdot I_{out(pulse)} = \frac{V_{out}^2}{\eta_1 V_{FC(pulse)} R_{out(pulse)}} \quad (47)$$

The dynamic of the buck CVS converter is shown in phases plane (Fig. 7.56). The chaotifying effect is shown in a zoom, where the limit cycles are shown around the steady-state point of (25V, 25A). The simulations are performed for the 6 kW PEMFC with a fuel flow rate of 47 lpm, which set the MPP at approximately 120 A and 50 V. Considering the RF of the output voltage as before, i.e. 4%, the CVS controller can be designed in the same manner. Thus, considering a switching frequency of 10 kHz, the HPS parameters are $L_1 = L_2 = L = 200$ μH and $C_f = 100$ μF, so $f_{LC} = 1.1254$ kHz. The performance indicators are shown in Table 7.8 for different load currents. These results validate the following conclusions: (1) the design of the CVS controller is less dependent to the load power level and (2) the performances regarding the voltage ripple and the spreading of the power spectrum are maintained for different load power levels in range. The restriction to power level means that the associated frequencies of the buck CVS converter (f_{RL} f_{LC} and f_{RC}), the saw-tooth frequency (f_{sw}), and the closed loop frequency, f_0, must verify the equation (48):

$$\max(f_{RC}, f_{RL}, f_{LC}) < f_{sw} < f_0 \quad (48)$$

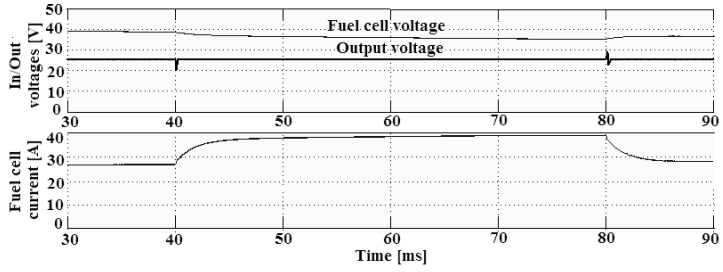


Fig. 7.55. The buck CVS tested with a pulse load current [33]

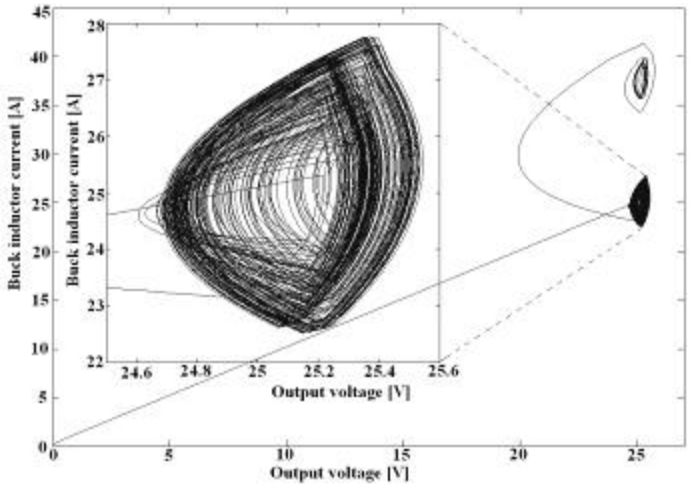


Fig. 7.56. The buck CVS dynamic in the phases plane [33]

Table 7.8. The performance indicators for a 6 kW PEMFC / 200 Ah battery HPS [33]

I_{out} [A]	f_{RL} [kHz]	f_{RC} [kHz]	PI_1 [%]	PI_2 [%]	RF_{Vout} [%]
20	1.9894	0.636	47	50	4.5
40	0.994	1.2732	37	44	3.7
60	0.663	1.9099	28	45	3.5
80	0.497	2.5465	30	41	3.8
100	0.397	3.1831	32	49	4

In this chapter the MPP was considered as an operating point for the PEMFC stack. If the load is dynamic, having an unknown power profile, then the load following control loop must be used to set the fuel flow in correlation with the requested power. As it is known the MPP tracking process is relatively slow, the searching time being dependent to the MPP algorithm chosen and to the PEMFC time constant [44, 45]. A new HPS topology was proposed and analyzed. The multi-port topologies are proposed to overcome the issues that usually appear in hybrid vehicle applications [46, 47]. In this chapter a multi-port topology of bi-buck type is proposed to mitigate the inverter ripple based on a buck CCS that generates an anti-ripple.

In this last section, the buck CVS is presented. The design goal for the CVS controller is to regulate the output voltage and reduce the electromagnetic interferences. The RF of the output voltage is up to 4% even if the anti-control technique is used to spread the power spectrum. The spreading in the HF band of the LF ripple, which remains after active compensation via the buck CCS, leads to an increase of the PEMFC life cycle as well.

Two performance indicators are used to quantify the spreading level of the power spectrum. The first one is a measure of the width of the frequencies band

where the most part of the power spectrum is situated. The second one is a measure of the peaks level in the power spectrum.

The proposed nonlinear CVS controller is designed to assure the best performances in both frequency and time domain. All the reported results have been validated in several simulations. The following performances are obtained: a RF of the output voltage up to 4% for the load current in the rated range, about 3 - 37 kHz width for the frequencies band of the spread power spectrum, and power peaks in range of 30 to 55 % from THD.

7.6 CONCLUSION

The LF current ripple appears in the normal operation of the FC inverter system and this is propagated back via the power converters to the PEMFC stack. Also, in FC vehicle applications, high energy demands appear in a short time. That will cause high current pulses with high slopes, which are propagated back as a LF current ripple, too.

In this chapter, the bi-buck topology is analyzed as a multi-port topology for the FC HPS. The bi-buck converter was designed to mitigate this LF current ripple via a buck CCS that will inject an anti-ripple into the point of the common coupling. In this node the dynamic load, the buck CVS and the buck CCS are connected. The anti-ripple is generated to track the shape of the LF inverter current ripple based on an active control implemented in the CCS controller. The use of a nonlinear control law improves the mitigation performances.

The buck CVS is used to spread the LF ripple that remains after active compensation. For high power HPS applications, the buck CVS can be removed to increase the HPS efficiency. The FC stack can operate under a dynamic load near the MPP by setting the fuel flow rate via a load following control and a MPP tracking control. For a dynamic load it is necessary to assure the power balance by adding an ESD (mixed stack of batteries and ultracapacitors) on a low or a high voltage bus. In the last case a bidirectional converter is necessary.

Some state-of-art architectures for the FC HPS are showed in this chapter. For the analyzed HPS architectures nonlinear control laws that can effectively mitigate the current ripple to a RF of approximately 3% (better than the RF reported in the literature), without increasing the voltage ripple factor over 4%, were proposed.

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